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ISSN 2475-742X

CPSS Transactions on Power Electronics and Applications

VOLUME 2 NUMBER 3 SEPTEMBER 2017

INAUGURAL SPECIAL ISSUE ON THE DEVELOPING TRENDS OF POWER ELECTRONICS: PART4

A PUBLICATION OF THE CHINA POWER SUPPLY SOCIETY

CPSS TRANSACTIONS ON POWER ELECTRONICS AND APPLICATIONS

CPSS Transactions on Power Electronics and Applications (CPSS TPEA) is sponsored and published by China Power Supply Society and technically co-sponsored by IEEE Power Electronics Society. It publishes original and high quality peer reviewed papers in the field of power electronics and its applications. With the goal of promoting the technology of power electronics including concepts, theory, modeling and control, analysis and simulation, emerging technology and applications, CPSS TPEA is expected to be a favorable platform to strengthen information exchange in this area. Interested authors are welcome to submit your papers via the Manuscript Central (https://mc03.manuscriptcentral.com/tpea-cpss) online submission system. You can find more information on our website: http://tpea.cpss.org.cn.

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Editorial for the Inaugural Special Issue on the Developing Trends of Power Electronics: Part 4

WITH this editorial, we sincerely welcome our readers to the brand-new publication — CPSS Transactions on Power Electronics and Applications (CPSS TPEA). It is sponsored and published by China Power Supply Society (CPSS) and technically co-sponsored by IEEE Power Electronics Society (IEEE PELS).

CPSS was founded in 1983 and has been the only top-level national academic society in China that solely focuses on the power supply/power electronics area. In the past 30-plus years CPSS has dedicated to provide to its members, researchers, and industry engineers nationwide with high quality services including conferences, technical training, and various publications, and this in deed has helped the society build up its membership rapidly, which now totals up to more than 4000 individual members plus 500 enterprise members. The fast growth of membership in turn compels CPSS to always work out better services for its members, one of which being the open-up of this periodical — a new journal in English language as a publication platform for international academic exchanging. This of course needs to be done through international cooperation, and that's why IEEE PELS is tightly involved, being the premier international academic organization in power electronics area and one of the fastest growing technical societies of the Institute of Electrical and Electronics Engineers (IEEE).

To fulfill the publishing need of the fast-developing power electronics technology worldwide is a more important purpose of launching this new journal. So far there are only 3 or 4 existing journals which are concentrated on power electronics field and have global reputation. For quite a few years people in the international power electronics community have had the feeling that, the existing journals have not even come close to meeting the huge demand of global academic and technology exchanges. E.g., the two existing IEEE power electronics journals, i.e. IEEE Transactions on Power Electronics (IEEE TPEL) and IEEE Journal of Emerging and Selected Topics in Power Electronics (IEEE JESTPE), now publish about 1000 papers a year, which is under a very low paper acceptance rate of around 25%, but still have a back-log of about one year for the newly accepted papers to finally appear in printed form to the public. The addition of this new dedicated journal would be an ideal improvement to fulfill such a tremendous need.

The booming of publishing need really is an indicator of how fast power electronics has been developing in recent years. Innovations have been continuously coming up from component (both active device and passive device), module, circuit, converter, to system level, covering different technical aspects as topology or structure conceiving, modeling and analysis, control and design, and measurement and testing. New issues and corresponding solutions have been continuously presenting as the applications of power electronics prevail horizontally in almost every area and corner of human society, from industry, residence and commerce, to transportations, and penetrate vertically through every stage of electric energy flow from generation, transmission and distribution, to utilization, in either a public power grid or a stand-alone power system. I personally believe that we are entering a world with "more electronic" power systems. The prediction around 30 years ago, that power electronics one day will become one of the major poles supporting the human society, is coming into reality. And I also believe, that power electronics is going to last for long time as an important topic since it is one of the keys to answer a basic question for human society, which is how human can harness energy more effectively and in a manner friendlier to both the user and the environment.

Therefore, I assume that there is probably no better fitting as for CPSS TPEA to publish its first few issues under a special topic about the developing trends of power electronics. We have invited a group of leading experts in different areas of power electronics to write survey/review papers or special papers with review/overview nature to some extent. To publish in a timely and regular style, we organize this inaugural Special Issue into different parts. Part 1, 2 and 3 were published in the December issue last year, the March issue and the June issue this year respectively, Part 4 appears in this September issue, and the last part is scheduled for the December issue.

In Part 4 we are honored to have 6 invited papers. The first three all address topics tightly related to wide-bandgap devices, from design and packaging to applications. The next two follow up with the state-of-the-arts in the motor drives area, and the last one deals with modulation techniques for multi-level inverters.

We begin with a paper on the silicon carbide power electronics design. It is authored by Dr. Alan Mantooth and his research group from the University of Arkansas. It describes recent advances of the research on the SiC-device-based power electronics, covering different aspects like integrated circuit design, semiconductor device modeling, 3D electronic packaging, and computer-aided design. These emerging trends really are leading to additional improvements in power density and more feasible operation at extreme temperatures.

The second paper provides a review on the SiC power

module packaging. It is written by Dr. Yong Kang and his research group from Huazhong University of Science and Technology. It presents a broad overview of the advanced module packaging techniques for SiC devices from module layout, packaging material system, up to module integration trend. The main challenges and potential solutions for the packaging of SiC modules are discussed.

The third paper is about the application of GaN devices to the totem-pole bridgeless AC-DC converter beating the traditional Si-based boost PFC. It is written by Dr. Alex Q. Huang and his research group, who recently moved to the University of Texas at Austin. It reviews the key technologies and designs for both hard-switching and soft-switching GaN totem-pole PFC indicating that the high frequency soft-switching solution is more preferable to achieve both high efficiency and high power density.

The fourth paper is written by Dr. Thomas M. Jahns and his research group from the University of Wisconsin-Madison, regarding the physical integration of power electronics and electric machines. The paper examines the future of integrated motor drive (IMD) technology by first reviewing the history of IMD products from the 1960s to today. A long-term vision for IMDs is then presented in detail, showing that wide-bandgap power semiconductor devices and a variety of other promising technologies are critical to realizing the full potential of IMDs.

The fifth paper is written by Dr. Ralph Kennel and his research group from the Technical University of Munich, discussing advanced control strategies for direct-drive PMSG wind turbine systems. It reviews and evaluates four control solutions in terms of their theoretical backgrounds, implementation approaches and control performances. The realizations and experimental assessments are also carried out with comprehensive evaluation results included in the end.

Last but not least, the sixth paper is written by Dr. Yongdong Li and his research group from the Tsinghua University in Beijing. The paper summarizes and compares five different space-vector Pulse Width Modulation (SVPWM) techniques for multilevel inverters. It turns out that the technique which the authors call SVPWM based on imaginary coordinate is the simplest in implementation and provides a better control on zero-sequence component than the other four.

I'd like to thank the authors of all these 6 invited papers. It's their high-quality contributions that finally leads to the launching of this new journal. I'd like to thank Dehong Xu, President of CPSS, who in 2015 initiated the idea of publishing the new journal and since then has been persistently supporting my work as the founding Editor-in-Chief. I'd also like to thank Jiaxin Han, Secretary General of CPSS, Jan A. Ferreira, President of IEEE PELS, 2015-2016, Don F. D. Tan, President of IEEE PELS, 2013-2014, and Frede Blaabjerg, IEEE PELS Vice President for Products, 2015-2018, who form the CPSS and IEEE PELS Joint Advisory Committee for our new journal with Dehong Xu and myself. Other IEEE officers and leading staffs like Dushan Borojevich, PELS President, 2011-2012, Alan Mantooth, PELS President, 2017-2018, Mike Kelly, PELS Executive Director, and Frank Zhao, Director of China Operations, IEEE Beijing Office, just to name a few, also provided continuous support and constructive advices. My earnest thanks also go to the CPSS Editorial Office led by Lei Zhang, Deputy Secretary General of CPSS, for their wonderful editing work. It would not have been possible to create a new journal in such a short time without their efforts. I'd like to finally thank all the members of the Executive Council of CPSS and particularly the leaders of Chinese power electronics industry. They always firmly stand behind CPSS TPEA and ready to help whenever needed.

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Jinjun LIU received his B.S. and Ph.D. degrees in Electrical Engineering from Xi'an Jiaotong University (XJTU), China in 1992 and 1997 respectively. He currently holds the position of XJTU Distinguished Professor of Power Electronics, sponsored by Chang Jiang Scholars Program of Chinese Ministry of Education.

Dr. LIU coauthored 3 books (including a textbook), published over 200 technical papers in peer-reviewed journals and conference proceedings, and holds more than 30 invention patents (China/USA). He received for 7 times governmental awards at national level or provincial/ministerial level for scientific research achievements or academic/teaching career achievements. He also received the 2006 Delta Scholar Award, the 2014 Chang Jiang Scholar Award, the 2014 Outstanding Sci-Tech Worker of the Nation Award, and the IEEE Transactions on Power Electronics 2016 Prize Paper Award. His research interests are power quality control and utility applications of power electronics, micro-grids for sustainable energy and distributed generation, and more/all electronic power systems.

Dr. Liu has served as the IEEE Power Electronics Society (PELS) Region 10 Liaison and then China Liaison for 9 years, an Associate Editor for the IEEE Transactions on Power Electronics for 9 years, and starting from 2015 the Vice President for membership of IEEE PELS. He is on Board of China Electrotechnical Society (CES) and was elected to a Vice President of the CES Power Electronics Society in 2013. He is the Vice President for International Affairs, China Power Supply Society (CPSS) and the inaugural Editor-in-Chief of CPSS Transactions on Power Electronics and Applications.

Emerging Trends in Silicon Carbide Power Electronics Design

H. Alan Mantooth, Tristan Evans, Chris Farnell, Quang Le, and Robert Murphree

***Abstract*—The emergence of wide bandgap power semiconductor devices has opened the possibilities of improved electrical performance and power density. Advanced research into wide bandgap power electronics also includes advances in integrated circuit design, semiconductor device modeling, 3D electronic packaging, and computer-aided design of wide bandgap based electronics. These emerging trends are described along with some early results indicating the additional improvements possible in power density. Operation at extreme temperatures also becomes more feasible.**

***Index Terms*—Gallium nitride, power integrated circuits, power semiconductor devices, power electronics, silicon carbide, wide bandgap semiconductors.**

I. Introduction

WIDE bandgap power semiconductor device technology has become a key enabler for the miniaturization of power electronic systems. This fact has been described and demonstrated in the literature for the past decade or more for many applications. A search of the literature in IEEE Xplore alone reveals over 40,000 articles on wide bandgap related activities alone! Of these, hundreds would be focused on applications exclaiming the virtues of using SiC MOSFETs, JFETs, diodes, SJTs, and IGBTs. Over a similar timeframe investigators at Purdue, Cornell, NASA Glenn, GE, Arkansas, and KTH Stockholm have demonstrated integrated circuitry in silicon carbide (SiC) [1]-[11]. These circuits have been analog, mixed-signal, or digital and have been realized in a variety of technologies including bipolar, JFET, nMOS and CMOS.

A primary motivation for the desire to utilize SiC integrated circuits as opposed to silicon or silicon-on-insulator is revealed in high power density packaging efforts. Attempting to compactly package gate drivers, protection circuits and maybe even controllers with the power devices yields a desire to have circuitry that accommodates the junction temperatures produced by the SiC power devices. In some packaging architectures, shown later in the paper, orienting the gate driver on top of the power device is the ultimate in lower gate-loop and maybe even power-loop inductances to achieve clean switching waveforms. As such, a perfect coefficient of thermal expansion (CTE) match between the two die relieves the stress on the interconnect used between the power die and the integrated circuit die leading to longer term reliability – a fact that MUST be addressed as part of high power density, heterogeneous integrated design activity.

In order for all-SiC systems to be fully realized, where the term "all" refers to not only the power devices but also the integrated circuitry, several aspects of the design space must be simultaneously considered. These design flow issues will be described in Section II and include optimization, circuit analysis and modeling, as well as board level analysis and modeling. In many higher power systems, it also involves power module design and system assembly design and analysis. All of these issues together constitute a change in design thinking from traditional silicon based power electronics design.

As will be described in Section II, circuit analysis prior to circuit fabrication is an important element in any electronics design process. Circuit analysis relies on accurate models of the components in the circuit in order to produce results that predict the behavior of the circuit under a variety of electrical and environmental conditions. Section III describes the importance of semiconductor device models to the design process.

Section IV describes some of the SiC integrated circuits recently developed for all-SiC power converters and applications. These circuits represent a few of the key functions needed.

II. Design Automation for SiC Systems

Power electronics design is becoming increasingly multi-disciplinary with the advent of wide bandgap (WBG) devices. The ability for silicon carbide and gallium nitride devices to switch so fast has brought more simultaneous issues into play in order to fully realize the potential of these more ideal switches. These devices can operate at higher junction temperatures, which promotes higher reliability if proper thermal management is designed in. These devices can switch faster, so they allow the size of passives to decrease. Also, because of the faster switching, circuits are more prone to parasitics that can cause excessive ringing in voltage and current waveforms and unwanted electromagnetic interference generation. So, it is apparent that these WBG technologies promote miniaturization of power electronics [12].

Due to these trends toward higher power density and miniaturization, power electronics is entering a phase of greater integration. And, this integration is increasingly heterogeneous as defined by efforts to embed passives, integrated low-voltage circuitry, and sensors into the same package, board, or module platform with the power semiconductor devices. This integrative activity and the desire of many to optimize the design

Manuscript received September 14, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00016

tradeoffs demands new design automation tools [13]-[15].

A typical model-based engineering design flow for integrative systems is shown in Fig. 1 [16]. The V-diagram essentially begins in the upper left with the system requirements capture into an executable form. From here the process descends into a partitioned set of subsystems that are successively themselves partitioned and individually designed and verified. The V-diagram is then ascended on the right-hand side to ensure that what was designed meets the subsystem(s) and system specifications. This design approach has been applied to thousands of systems ranging from airplanes to cell phones. Power electronic systems are no different. In fact, as their complexity is increasing, appropriate tools for the various analysis, verification and validation steps required in the V-diagram must evolve or be created.

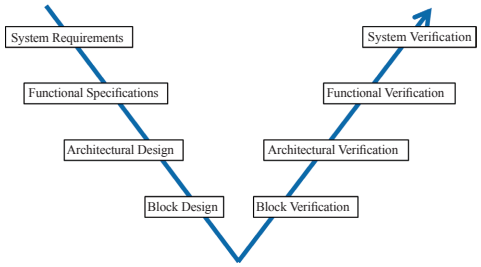

Fig. 1. The V-diagram design flow that represents a top-down specification and partitioning of a system and a bottom-up verification of the proposed designs. This approach allows for specification negotiation and helps to ensure first-pass success.

In the design flow of Fig. 1, as applied to traditional silicon power electronics in a systems such as more electric aircraft, electric cars, electric ships or hybrid heavy equipment, the typical toolset in today's terms would involve Matlab/Simulink® for some higher-level system analysis, controls development, and even some more idealized circuit analysis (often coupled with the control algorithms). It would involve a SPICE-like simulation tool such as LTSpice™, PLECS®, or Saber® for circuit analysis. Board level layout and analysis would be performed by any number of tools, but most would not typically possess proper signal integrity analysis capabilities Further, if the design called for power modules, then these are taken off the shelf with, at best, some equivalent model of the parasitics associated with the module.

With silicon carbide devices, higher switching frequencies, and higher power densities, this toolset is simply not rich enough. Thermal considerations are a first order concern. Electrical parasitics present in both the power modules and on the printed circuit boards must be accounted for or the circuitry simply may not work. In fact, WBG module design often needs to be tailored to the application to maximize performance and reliability. In the absence of advanced tools, this will lead to a degree of customization that results in expensive design and slow the adoption of the technology.

A. Circuit Analysis and Modeling

Circuit analysis tools have incrementally evolved over the past 45 years since SPICE was introduced by UC Berkeley in the 1970s. Clearly, engineers have for decades made due with macromodels and inferior device models for power electronics. The introduction of Saber in the late 1980s began to change this and open up the possibility of having analysis algorithms and models more suited to power electronics [17]. More will be discussed about semiconductor device models in Section III. Some degree of algorithm generalization in terms of integration order and type more ideally suited to periodic sinusoidal systems was introduced in Saber.

Research into switching circuit modeling techniques was also developed through the 1990s as well [18]-[20]. Other research into switching systems simulation was investigated, but found most of its applications in the digital domain [21]. State-space formulations have been advocated here and there through time, but none seem to find their way to mainstream tools. More recently PLECS has taken hold for power electronics as a commonly used tool. All of these approaches remain viable for WBG design, but perhaps it is time for a new formulation. One that is more dedicated to the nature of switching converters, and is more amenable to the design optimizations that the community seeks to achieve.

A comprehensive description of circuit analysis is a standalone topic for a manuscript or book. The main point to make in the context of this paper is that while the field of circuit analysis has matured, there is room for additional tools that may help to advance the multi-dimensional design tradeoff space that power electronics designers seek to command. A tool that runs fast, gives fairly accurate results, and can account for electrical, thermal, and electromagnetic issues.

B. Board Level Design and Analysis

One of the major benefits of using SiC devices is the remarkably low switching losses associated with these devices. This is in part due to their significantly faster transition times which minimizes the time in which the device is in the triode region of operation and reduces switching losses. Due to these fast switching characteristics and associated high *dv/dt* of SiC devices, power electronics designers are now required to factor board parasitics into their design process in a way similar to that of RF and high-speed digital circuit designers. In the past, power electronics designers were accustomed to working with frequencies in the 4 kHz to 20 kHz range with relatively low *dv/dt* (say 5 kV/μs depending on the device). These relatively slow transients allowed many of the board parasitics to be considered negligible by designers. With the emergence of SiC and other WBG devices, it is now possible, and routinely beneficial, to increase the fundamental switching frequencies from the single kHz range to the 100s of kHz range, and associated *dv/dt* transients in the 10-100s of kV/μs range, which allows for capacitors and inductors to be much more effective filters, at the frequency of interest, while also significantly reducing their size and weight. By this same line of reasoning, the once negligible board and trace parasitics can have an overwhelming negative effect on circuitry, and must be analyzed to mitigate adverse effects such as ringing, crosstalk, and conducted or radiated

electromagnetic interference (EMI).

In order to appropriately analyze the effects of board parasitics on the circuits associated with power electronics applications, a new iterative PCB design flow was developed and implemented. Fig. 2 shows the iterative design process currently used in the University of Arkansas (UA) power electronics groups.

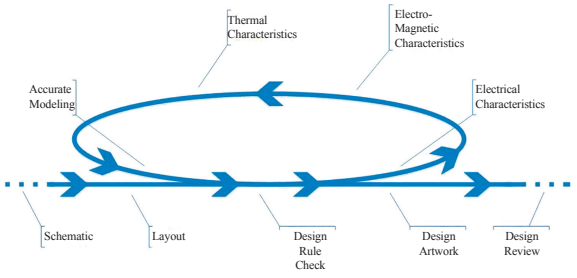

Fig. 2. Progression of general design flow illustrating iterative modeling process.

As a first step the circuit schematic is created and simulated using OrCAD™ PSpice, LTSpice, or PLECS tools to verify ideal operation. Once basic functionality of the circuit schematic is achieved the printed circuit board (PCB) layout is accomplished using Cadence Allegro™. At this point in the process it is common for power electronics engineers using silicon devices to verify certain "best practices" have been implemented during a design review and have the PCBs be sent out for fabrication. In our design flow we instead continue our analysis by exporting the generated board files to ANSYS SIWave™ and perform a parasitic extraction. Fig. 3 shows an impedance scan of a non-ideal PCB layout using SIWave.

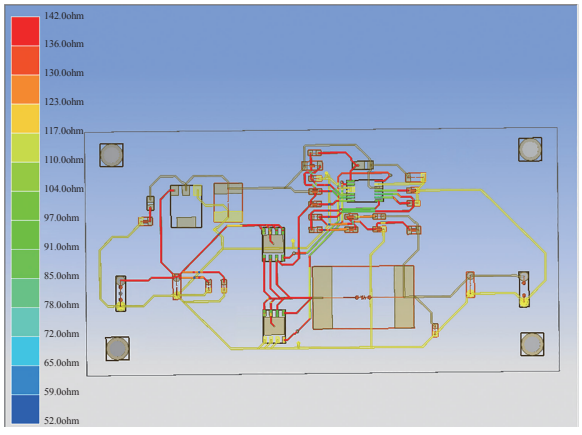

Fig. 3. Impedance scan of a non-ideal PCB layout.

Once the parasitic analysis has been completed using SIWave™ it is then exported to a PSpice circuit library which can then be incorporated into either the original OrCAD simulation or, for more advanced control algorithm evaluation, it may be imported into an OrCAD/Matlab-Simulink co-simulation environment that allows for a coupled controls-circuit simulation of the engineer's design.

With the circuit now available in the ANSYS tool suite, more advanced analysis may also be performed. The high *dv/dt* and *di/dt* switching characteristics of SiC and other WBG devices contribute significantly to radiated EMI that can adversely affect a product's compliance with FCC standards. It has also been observed that this radiated EMI can cause significant corruption of analog-to-digital converters (ADCs), gate drivers, and even controllers such as digital signal processors (DSPs) that have, in turn, caused catastrophic device failures (Fig. 4). By accurately modeling the circuit's conductive traces, along with high fidelity device modeling, an accurate representation of any transmission paths acting as antennas may be identified and subsequently mitigated. Fig. 5 shows the near-field simulation results for the example non-ideal PCB shown above.

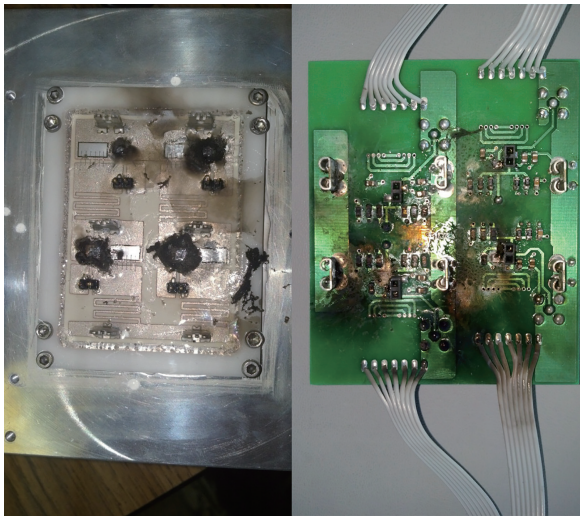

Fig. 4. Destroyed SiC power module (left) and gate driver board (right) due to EMI coupling back into the gate drivers and falsely triggering a power device leading to a shoot-through condition.

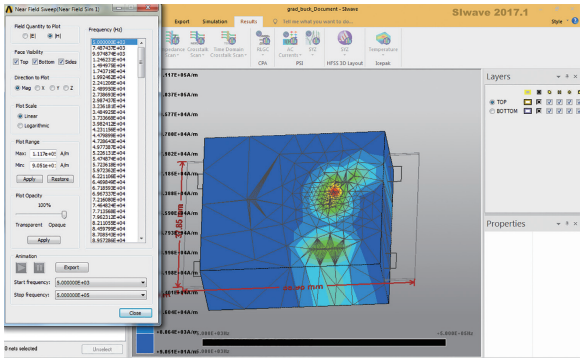

Fig. 5. Near field simulation results and frequency window as produced by SIWave.

Once all analyses have been completed for this base iteration, subsequent improvements and iterations are performed until all design specifications are met and the designer has a high confidence interval of success. This iterative process is analogous to the layout, extraction, analysis, and verification approach used in integrated circuit design prior to submission for fabrication.

C. Power Module Design

Reiterating, as the state of WBG devices advances, so too must the design and manufacture of power electronic modules in order to achieve greater power density. The higher operating temperature afforded by next-generation power semiconductors can reduce the cooling requirements, thereby reducing the overall size and weight of a system. Likewise, higher switching frequencies offered by these devices directly correlates to a reduction in both the size and weight of system-level passive components [12], [22]. Furthermore, integration of some of these passive components inside the module can have a profound impact on power density. For example, incorporation of decoupling capacitors allows for low impedance paths for parasitic current oscillation, mitigating some of the drawbacks of high frequency operation [23]. However, there are several limitations of conventional packaging techniques that are hindering the adoption of WBG devices. This includes not only the physical limitations of the materials chosen for packaging, but also geometrical considerations that a designer must carefully consider.

Among some of the most profound issues a power module designer faces are those related to parasitic inductance. These stray inductances in both the commutation and gate-source loops of power modules can cause several problems. The high operating frequency of WBG devices along with their high slew rates can lead to scenarios where a high *di/dt* leads to large voltage overshoots during switching transients. This overshoot reduces the safe operating area of the module and is a contributor to EMI issues [22], [24]. Additionally, gate-loop inductance limits the gate-source voltage rise and fall times which, in turn, increases transient duration and switching losses [25]. These can sometimes even end in catastrophic failure of the module as seen in Fig. 4.

This high *di/dt* and *dv/dt* associated with the fast switching of WBG devices is a major contributor to conducted and radiated EMI. Any methods employed to reduce stray parasitics in the module will have a direct impact on this. Research in this area by incorporating 3D packaging techniques has shown reduction in EMI as well as the benefits associated with a 3D structure. These include higher power density and the possibility for double-sided cooling [22], [26], [27]. Fig. 6 shows an example of a next-generation 3D, wire bondless module.

While the attractive thermal properties of WBG devices offer the possibility of higher device reliability and thermal capability, this does not guarantee the reliability of the system around these devices. Therefore, high reliability at high operating temperature is a crucial consideration. High temperature relates directly to system reliability in the form of failure mechanisms such as die attachment fatigue or bondwire cracking due to power and thermal cycling under harsh operating conditions [28], [29]. Delamination of direct-bonded copper (DBC) during extreme temperature cycling is another well-known failure mechanism that can be mitigated using the step-edge approach for the copper trace to reduce the thermal stress [30]. Undoubtedly, mitigation of these failure mechanisms will improve the reliability of the overall system. Therefore, detailed analysis is essential in the design phase.

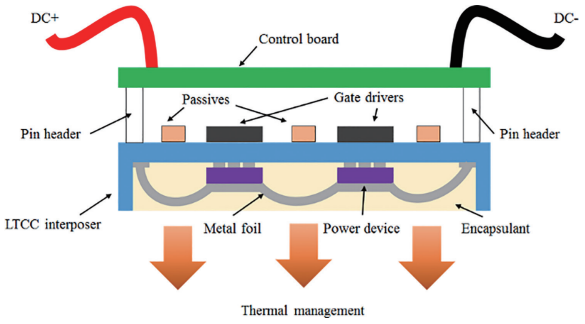

Fig. 6. A 3D power device and gate driver arrangement that significantly reduces generated EMI.

Due to the multidisciplinary nature of power module design, the abovementioned design objectives must be analyzed simultaneously in the design process. Presently, state-of-the-art methods employing high fidelity numerical simulations in an iterative loop are used to simultaneously analyze and synthesize reliable power module designs [31], [32]. While such techniques ensure high accuracy, they are usually computationally expensive, increasing evaluation time and reducing design flexibility. Alternatively, early work in [33] has employed thermal simulations along with lifetime analysis in a response surface based multi-objective optimization routine. This has reduced the number of simulations needed in search of an optimized design. Furthermore, the work in [34] has used strategies borrowed from VLSI work to develop an efficient automated design algorithm. An approach from [35] has shown fast and accurate design by employing reduced order modeling in an optimization loop. Most recently, the work in [36] has allowed more flexible parametric design using thermal resistance networks and closed form equations for both thermal and mechanical analysis. Overall, the abovementioned efforts for CAD tools, models, and algorithms have shown a promising future for a mature design automation flow for power electronic modules – even those that would be heterogeneously integrated with drivers, protection circuits, sensors, and passives where appropriate.

D. System Assembly Design and Analysis

One of the existing gaps in design automation for power electronics is cabinet-level design. Once the boards, modules, and subsystems are designed, then the task of design and layout of the cabinet is required. This includes electrical and thermal considerations as well as relevant standards pertaining to the application space such as industrial drives, electric grid, and automotive. Best practices and design tools have been identified as a need by engineers in the switchgear industry in particular.

III. Semiconductor Device Modeling

One of the emerging trends in SiC power electronics is the development of low-voltage SiC circuitry to be packaged with the SiC power die. One of the keys to being able to realize

accurate simulations of SiC circuits is accurate semiconductor device models. This is true for the power electronic circuit analysis [37], [38] as well as the low-voltage circuitry.

Designing integrated circuits depends heavily on the transistor models. Much effort is spent creating models that reflect all of the key characteristics of the transistors used in IC design. The models are typically charge-conserving so that all charges and resulting nonlinear capacitances are accurately modeled over bias and temperature. The models are typically non-quasi-static and capture the effects of bandgap voltage, mobility, and a host of observed physical phenomena [39]. The models are geometry scalable and temperature scalable within a certain regime. And, statistical and variability behavior is modeled so that Monte Carlo analysis and process corner evaluations can be performed in order to center and tolerance the designs. This level of precision engineering is necessary to create the applications we enjoy today in communications, consumer electronics, and computing. The power electronics industry does not enjoy this level of sophistication in its design procedures and levels of automation as outlined in the previous section. And, until WBG power electronics came along, one could argue it was not necessary for most applications. That situation is changing however.

Several generations of silicon transistor models have been created by a number of groups around the world as process technology marched from barely submicron to nanometer scales. Some of the most oft-used of these models are the Berkeley Short-channel IGFET Models (BSIM).

In the IC design world, the industry came together to standardize on compact models as these transistor models are known. After some investigation, the UA device modeling team chose the BSIM4 standard model to make modifications to in order to create a low-voltage SiC MOSFET model for both *n* and *p* type devices [40]. This new model known as BSIM4SIC has all of the features of BSIM4, but with appropriate modifications for SiC. The enhancements which are related to the SiC MOSFET are implemented in the Verilog-A version of the BSIM470. Those enhancements include:

- Non-silicon substrate and non-SiO_2 gate dielectric model using the model flag MTRLMOD. Assigning 1 to the parameter activates the new model,
- A new mobility model that includes the effects of Coulomb scattering resulting from the presence of interface trapped charge. The model can be selected by assigning 3 to the model parameter MOBMOD,
- Trap assisted leakage current modeling of the junction diodes,
- A new definition of effective gate-to-source voltage for the C-V model,
- Effective oxide thickness model for high-κ gate dielectric, electric and physical oxide thickness model to take into account the effects of process variation,
- A charge centroid model for quantum mechanical tunneling of inversion carriers into the oxide,
- A new temperature dependent bandgap model,
- Enhancement of the threshold voltage shift model due to pocket implant,

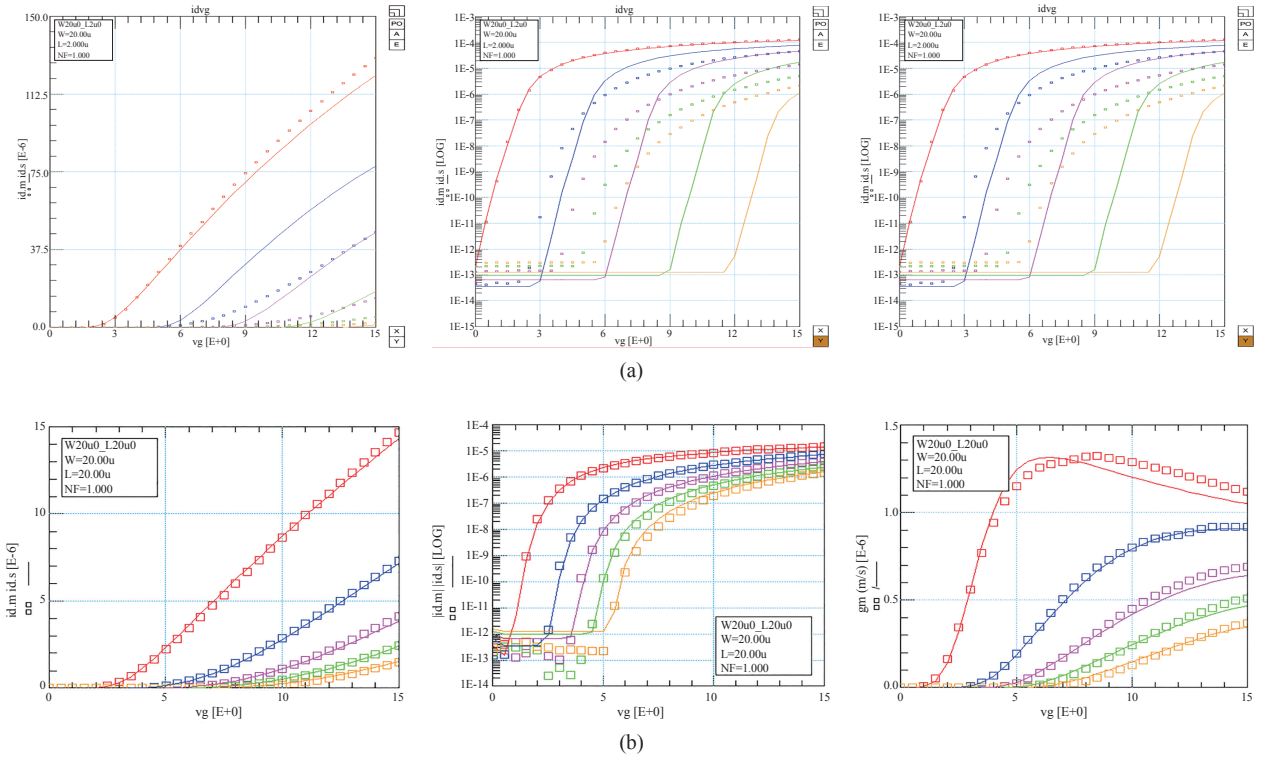

Fig. 7. The best fit curves for BSIM4 against nFET measured data illustrating the body effect (top curves left to right): drain current vs. gate voltage for various back gate voltages at low v_{ds}; drain current vs. gate voltage at high v_{ds}; transconductance (g_m) vs. gate voltage. The same curves for BSIM4SIC illustrating how well the new model can be fit to the measured data because it possesses the correct physics.

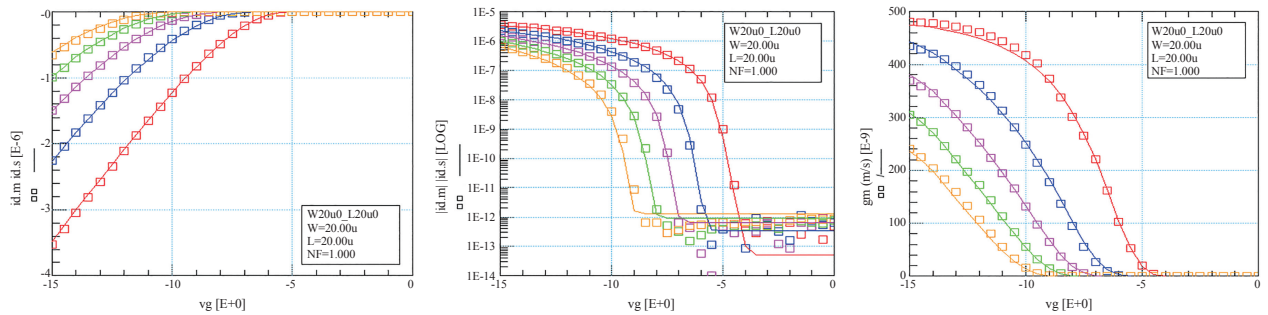

Fig. 8. The best fit curves for BSIM4SIC against pFET measured data illustrating the body effect (top curves left to right): drain current vs. gate voltage for various back gate voltages at low v_{ds}; drain current vs. gate voltage at high v_{ds}; transconductance (g_m) vs. gate voltage.

- A new body effect model,
- A new soft saturation (transition from triode to saturation) model,
- A new channel length and temperature dependent zero bias mobility model, and
- A new temperature scaling model.

Many of these effects including flat band voltage shift, mobility reduction, non-monotonic temperature behavior, soft velocity saturation, and the non-silicon-like body effect can be traced to interface trapped charge in SiC devices.

The results given in [40] show exhaustively how the new model compares to measured data and previous model versions. One example for illustration is the body effect modeling. Fig. 7 shows the best fit for the traditional BSIM4 model to the measured data of SiC devices and the fit for BSIM4SIC in part b. These results are for an nFET device, but similar results were obtained for a pFET (Fig. 8). These sample curves provide insight into the importance of the transistor models for IC design activity and are another example of a design automation component required to effectively pursue all-SiC power converters.

IV. SiC Integrated Circuit Design

The maturity of traditional silicon power process technologies has led to the nearly complete realization of silicon's potential. Fundamental limitations of silicon prevent it from keeping pace with the power electronics industry's growing demand for increasing power density and concomitant higher operating temperatures. As a result, there has been a notable market shift towards SiC and GaN power devices. These wide bandgap materials are advantageous in power electronics applications due to offering higher critical electric fields and thermal conductivity compared to silicon.

While SiC power devices are commercially available, the corresponding control and protection circuitry is currently silicon based. This introduces a limiting factor for the efficient operation of power modules, particularly at high temperatures since silicon and silicon-on-insulator (SOI) based devices are limited to approximately 125 °C and 250 °C, respectively [41], [42]. To operate in high temperature environments without a significant degradation in product lifetime, these circuits require dedicated cooling solutions that increase costs and add parasitic elements.

To realize the potential of wide bandgap power devices, packaging techniques and integrated circuitry must be developed with similar operational capabilities. With demonstrated operation at temperatures exceeding 300 °C, SiC CMOS ICs represent a viable approach to meeting these requirements [6]-[9]. Flip-chip packaging techniques allow for the realization of a 3D wire bondless power module in which the SiC CMOS gate driver, power management, and protection ICs connect to a power device using solder balls and an interposer. This reduces parasitic elements, yielding the potential for higher switching frequencies along with improved efficiency and reliability.

A. SiC Gate Driver

The SiC CMOS gate driver shown in Fig. 9 and presented in [6] has achieved operation above 400 °C with sinking and sourcing capabilities of 8 A and 4 A, respectively. As shown in Fig. 10, the design enables an adjustable drive strength by implementing multiple output stage splices that can allow for higher efficiencies when driving smaller loads. A fault detection feature was also incorporated due to yield issues experienced in previous SiC IC fabrication runs.

B. SiC Power Management and Protection Circuitry

The development of a SiC gate driver with features comparable to a commercially available silicon based counterpart will

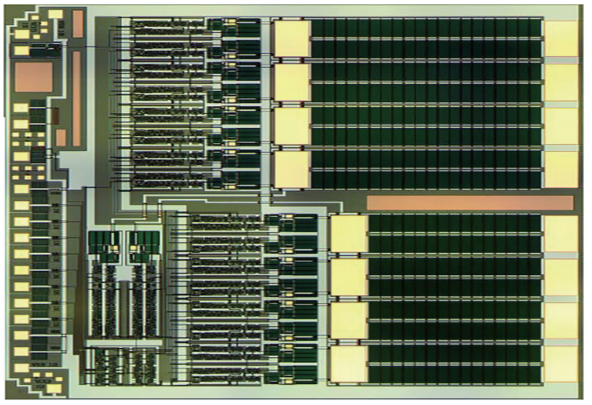

Fig. 9. A die micrograph of the SiC CMOS gate driver fabricated in the HiTSiC® process.

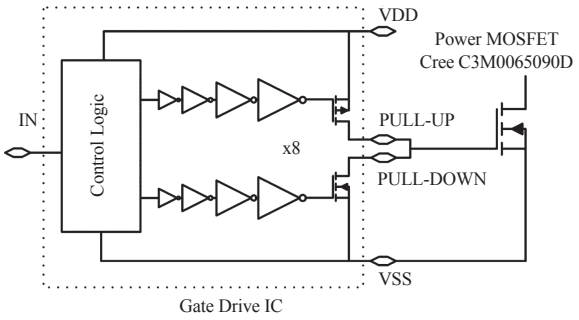

Fig. 10. The schematic of the SiC CMOS gate driver fabricated in the HiTSiC® process.

require an integrated voltage regulator and protection circuitry. The SiC CMOS linear regulator shown in Fig. 11 was designed and fabricated in the same process as the gate driver and is functional at over 400 °C [9]. The regulator provides an output voltage of 15 V from an input voltage of 20 V to 30 V and achieves a continuous output current of 100 mA. An all-NMOS SiC UVLO design has also been presented in [43] and provides a template for the necessary protection circuitry.

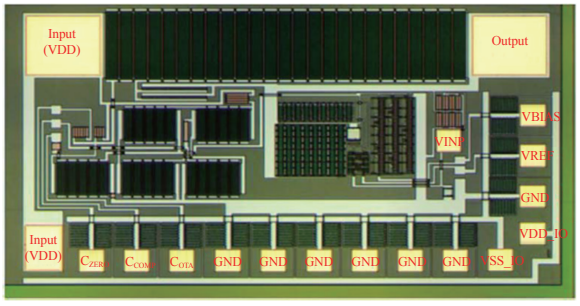

Fig. 11. A die micrograph of the SiC CMOS linear regulator fabricated in the HiTSiC® process.

C. Extending the State of the Art SiC IC Technology

A foundation of SiC CMOS designs has been established with a multitude of mixed-signal circuitry including op-amps, bandgap references, and data converters [8], [44]. More complex designs will be formed by building upon the experience gained in previous design and testing phases. In the case of op amps, for example, a shift towards a higher gain architecture such as the recycling folded cascode [45] will improve the load regulation of the linear regulator. This enhances the precision of the regulator output voltage for a given range of load currents, which can be critical in power electronics applications.

An offset cancellation scheme is another key to the progression of SiC ICs. By implementing this in conjunction with the op amp and bandgap reference in a linear regulator, a temperature stable output voltage can be achieved. The culmination of these efforts creates a path to a fully integrated, intelligent gate driver that provides functionality similar to commercially available silicon based parts while breaking the barriers to even greater power density.

V. Conclusion

Economy and performance are benefits that come with high power density power electronics, just as in the case of integrated circuit electronics. High density power electronics require the heterogeneous integration of disparate technologies including power semiconductor devices, driver, protection and control circuitry, passives and voltage isolation techniques. One of the keys to advancing power electronic integration has been the commercial reality of wide bandgap power semiconductor devices.

This paper described some of the key emerging trends in SiC power electronics design. One of these trends is in design automation tools for module and board layout, device modeling, parasitic extraction, and verification techniques to address fast switching WBG technologies. Gaps indeed exist in the power electronics design automation space, and advances will be needed to maximize performance. Another trend is wide bandgap integrated circuitry. While this paper focused on SiC, there are efforts on GaN IC design to couple it with GaN devices [46]. A key enabler for WBG IC design is semiconductor device modeling for low-voltage devices. This is another emerging trend [47], [48]. The ability to design and manufacture wide bandgap integrated circuits as drivers, controllers, and protection circuitry allows them to be packaged in close proximity to the power device die to minimize parasitics that would adversely impact system performance. More 3D packaging approaches are likely to be demonstrated as part of the effort to achieve low-inductance, high power density electronics.

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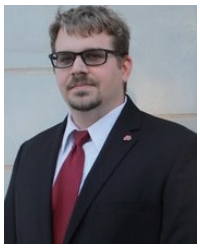

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A Review of SiC Power Module Packaging: Layout, Material System and Integration

Cai Chen, Fang Luo, and Yong Kang

***Abstract*—Silicon-Carbide (SiC) devices with superior performance over traditional silicon power devices have become the prime candidates for future high-performance power electronics energy conversion. Traditional device packaging becomes a limiting factor in fully realizing the benefits offered by SiC power devices, and thus, improved and advanced packaging structures are required to bridge the gap between SiC devices and their applications. This paper provides a review of the state-of-art advanced module packaging technologies for SiC devices with the focuses on module layout, packaging material system, and module integration trend, and links these packaging advancements to their impacts on the SiC device performances. Through this review, the paper discusses main challenges and potential solutions for SiC modules, which is critical for future SiC applications.**

***Index Terms*—Packaging material system, power module integration, SiC advanced packaging.**

I. Introduction

RAPID development in power electronics systems poses strong demand for better power semiconductor devices. Silicon (Si) device has been dominating in this area for decades, and now it almost hits the material theoretical limitations [1] for further improvement on the device's switching and conduction performances. Therefore, Wide Bandgap (WBG) material based devices start to attract attention of power electronics engineers.

Compared to Si power devices, WBG power semiconductors has lower intrinsic carrier concentration (10-35 orders of magnitude), higher electric breakdown field (4-20 times), higher thermal conductivity (3-13 times), and larger saturated electron drift velocity (2-2.5 times) [2]. Translating these characteristics into device specifications, given the same die size and thickness, WBG devices can provide higher breakdown voltage, higher current, higher operating temperature, higher switching speed and lower switching loss over Si devices. TABLE I [3], [4] summaries the figure-of-merit comparisons for WBG and Si devices, which shows that, theoretically, the performance of SiC and GaN devices surpasses that of Si devices regarding switching loss, switching speed and current density with orders of magnitude. However, these outstanding benefits cannot be demonstrated in power electronics converters on the same scale due to the packaging limitations [5]-[9]. Power device packaging, which is the bridge between power device and its application, has become a bottleneck for WBG device applications [10]. The challenges in SiC power module packaging are brought by the unique characteristics of SiC devices, which can be summarized in following aspects:

TABLE I
Main Figure-of-Merit Comparisons for WBG and Si Power Semiconductors

	Si	GaAs	6H-SiC	4H-SiC	GaN	Diamond
JFM	1.0	1.8	277.8	215.1	215.1	81000
BFM	1.0	14.8	125.3	223.1	186.7	25106
FSFM	1.0	11.4	30.5	61.2	65.0	3595
BSFM	1.0	1.6	13.1	12.9	52.5	2402
FPFM	1.0	3.6	48.3	56.0	30.4	1476
FTFM	1.0	40.7	1470.5	3424.8	1973.6	5304459

JFM : Johnson's figure of merit is a measure of the ultimate high frequency capability of the material.
BFM : Baliga's figure of merit is a measure of the specific on-resistance of the drift region of a vertical FET
FSFM : FET switching speed figure of merit
BSFM : Bipolar switching speed figure of merit
FPFM : FET power handling capacity figure of merit
FTFM : FET power switching product
BPFM : Bipolar power handling capacity figure of merit
BTFM : Bipolar power switching product figure of merits

A. High Switching Speed (dV/dt and di/dt)

Compared to Silicon devices, SiC device has much lower C_{oss} and Q_g, and they can switch at much higher *dV/dt* and *di/dt* [11]. High switching speed enables low switching loss and high switching frequency, which can potentially improve the converter power density and efficiency. Nevertheless, this new feature poses strong challenges for parasitic control. With the same amount of parasitic inductance, higher *di/dt* will generate higher voltage overshoot and ringing across the device, which can significantly increase the device switching losses, device voltage stresses and EMI noises. With the same amount of parasitic capacitance, higher *dV/dt* will result in higher common mode noise, which can increase the load for EMI filtering in converters.

High switching speed also brings challenges in device paralleling. Multi-chip parallel operating is an effective way for power scaling at the module level. Current balancing in both steady-state and dynamic region is the key design consideration

Manuscript received September 11, 2017. This work was supported by the National Natural Science Foundation of China under Grant 51507069.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00017

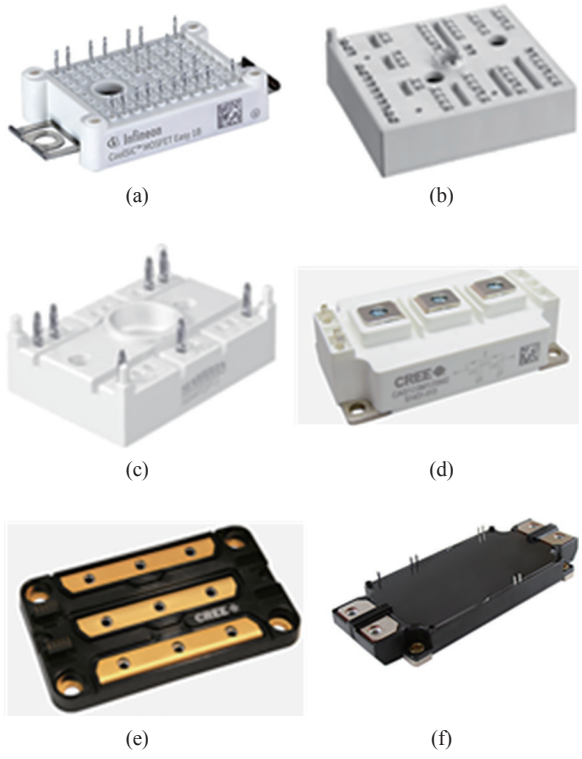


Fig. 1. Some commercial SiC power module packages: (a) Infineon Easy1B, (b) SEMIKRON MiniSKiiP, (c) SEMIKRON SEMITOP, (d) Wolfspeed 62 mm, (e) Wolfspeed high Performance 62 mm, (f) ROHM type C.

in device paralleling, which is usually realized by symmetrical layouts for the paralleled devices. High switching speed increases the sensitivity of parasitic symmetry makes it difficult to maintain current balance at high switching speed.

B. High Operation Temperature and High Electric-Field

SiC device provides the potential to achieve higher power density, which means the power package for SiC devices will also need to take much higher loss density. SiC device has the extraordinary capability for high-temperature operation up to 200°C -300°C. This temperature has been way beyond the suitable range for traditional packaging material systems for Si devices, which usually no higher than 175°C. It is important to search for new packaging material systems which can reliably sustain such a high-temperature operation.

For the same breakdown voltage, SiC device die is much thinner than SiC devices. This feature leads to challenges on the mechanical stability considerations for SiC power module packaging. Selections of appropriate substrates, die-attachment materials and encapsulation material to match with the thermal expansion coefficient of the SiC devices are the key factors to the success of SiC packaging.

Due to the same thin die thickness feature, to handle the same voltage, SiC device package will need to sustain higher electric field than that in Si power device packages. This new feature requires new insulation packaging materials to support in device applications.

In response to these challenges, this paper provides a review from three approaches including advanced module layout, material system selection and module integration. Each approach provides a solution to one or a couple of the challenges listed above. For a fair comparison, this paper firstly presents an overview of the state-of-the-art packaging approaches for commercially available SiC devices, and then this paper summaries the new advancement in research works for advanced packaging structure, packaging material systems and the module integration trend, from both academia and industry. The prospected trend for the future of SiC module packaging is included in the last part of this paper.

II. The State-of-the-Art for Commercially Available SiC Power Devices

Driven by the emerging market, SiC device manufactures tried best to pull available resources together to provide their products to meet users' demand. TABLE II and TABLE III list major SiC manufacturers with their product specifications [12]-[16], which present the state-of-the-art packaging for commercially available SiC power products, as summarized below:

SiC discrete devices are available from 650 V to 1700 V while maximum rated current is around 120 A. In this range, TO247/220/263 and SOT 227 packages are the dominating forms of power devices. There are varieties on the pin-configurations and Kelvin Gate structure in these traditional packages. However, the nature of TO and SOT packages introduce high parasitic power loop inductances (usually around 20-30 nH) and high thermal impedance, which reduces the benefit of using SiC devices [17].

SiC Power modules are commercially available from Wolfspeed, RHOM, GeneSiC, Infineon and SEMIKRON [18]-[22]. Both Wolfspeed and RHOM provide 2-level, half-bridge, and phase-leg modules. RHOM's module is in an EconoDual package, which is similar to the state-of-the–art IGBT package. Its packaging loop inductance is around 15 nH. Wolfspeed provides different packages from its product line for different applications. 63 mm standard packaged modules. This traditional package has been widely adopted by high power Si IGBT devices. It provides benefits of high technical maturity and low cost. However, this package also comes with obvious disadvantages including high parasitic loop inductance (15 nH- 20 nH), moderate thermal impedances and heavy packaging weight. These features can potentially limit the performance of WBG devices. To address those problems, Wolfspeed announced their new generation SiC modules in their new HT package. The new design has 9 nH power loop inductance with ultra-light weight and improved thermal management. These are enabling features to unleash the potential of WBG devices. The module from GenSiC consists of a single switch instead of a phase-leg. It is in SOT-227 package, which is a standard package for Si power switches. Infineon and SEMIKRON also launched new full SiC power module and the inductance can be reduced to 15 nH.

Commercially available packages support device junction temperature up to 200°C (from STMicroelectronics and CREE), most of the off-shelf modules stays with the same temperature range as Si modules (150 °C -175°C).

TABLE II
COMMERCIAL DISCRETE SIC DEVICES

Manufacturer	Wolfspeed				ROHM			USCi			STMicroelectronics	
Voltage (V)	900	1000	1200	1700	650	1200	1700	650	1200	1200	650	1200
Technology	SiC MOSFET				SiC MOSFET			SiC Cascode		SiC JFET	SiC MOSFET	
Package	TO247/ TO263	TO247/ TO263	TO247/ TO247	TO247/ TO263	TO247/ TO220	TO247	TO247/ TO268	TO247	TO247	TO247	TO247	TO247
Current (A)	11.5 - 36	22 - 35	10 - 90	5 - 72	29 - 118	10 - 95	6	20	20 - 35	21 - 38	100	12 - 65
Operating Temperature (°C)	150	150	150	150	175	175	175	150	150	175	200	200
C_{oss} (pF)	20 - 60	40 - 60	23 - 220	12 - 171	35 - 148	41- 237	19	178	57	53000	305	30 - 170
Ron (mΩ)	65 - 280	65 - 120	25 - 280	45 - 1000	17 - 120	22 - 160	750	45	60 - 100	45 - 80	22	69 - 690
Q_g (nC)	9.5 - 30.4	21.5 - 35	20.4 - 161	13 - 188	172	42 - 178	17	47.5	47.5	62	215	22 - 122

TABLE III
COMMERCIAL SIC POWER MODULES

Manufacturer	Wolfspeed		ROHM	GeneSiC	Infineon	SEMIKRON
Voltage (V)	1200	1700	1200	1200	1200	
Package	45mm/62mm/High Performance 62mm	62mm	Type C/E	TO247/SOT227/TO263	AG-EASY1B-2	MiniSKiiP/ SEMITOP/ SEMIPACK/ SEMITRANS
Current (A)	20 - 325	225	80 - 300	25 - 160	50 - 100	14 - 541
Operating Temperature (°C)	150 - 175	150	150 - 175	175	150	175
C_{oss} (pF)	100 - 2570	2500	2000 - 4000	>440000	470	NC - 1644
Ron (mΩ)	3.6 - 80	8	9.67 - 43.75	10 - 100	11 - 23	NC
Q_g (nC)	270 - 3200	4400	560 - 1500	55	62 - 250	NC - 2268

These two tables shows that most of the SiC power device manufacturers provide their SiC devices with traditional packages due to the low cost and timely market availability. Although the industry has been aware of the importance of power module packaging for SiC device, the demand on advanced power package has not yet been matched with its research and development.

III. ADVANCED PACKAGING STRUCTURES

A standard traditional power module package (as shown in Fig. 2, insert a picture here) includes a 7-layer structure, including a heat-sink, a base-plate, a DBC substrate, and die-attachments between these layers. The top side of the device is usually wire-bonded to external lead-frames, while the bottom side of the device is attached onto the DBC traces. The current flow in the device goes from the bottom contact vertically through the device and bond-wires to the terminals of the module. The module is often filled with encapsulation material to prevent the device and bond-wires from environment contamination/vibration. This module structure usually comes with high parasitic power loop inductance ranging from 20 nH to 30 nH.

As stated in the introduction, SiC device has high speed switching capability, which makes the device is sensitive to its packaging parasitics. Parasitic inductance in the power module

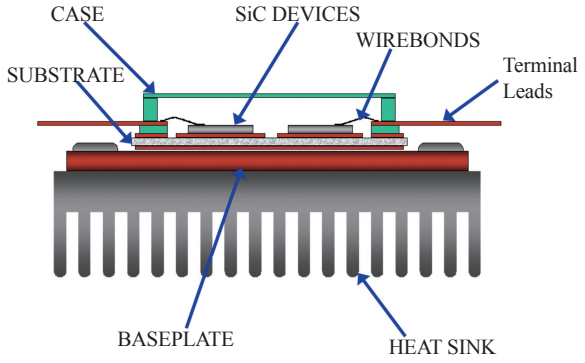


Fig. 2. The cross-section of a traditional wire-bonded power module.

induces high voltage overshoot and ringing on switching devices, which then increases the device switching loss [23] and EMI emission from the modules. Advanced packaging structure can significantly help to minimize of the loop parasitics by optimizing its current commutation loop layout within the package. Therefore, advanced packaging structure can sufficiently realize high efficiency and high frequency switching operation using SiC devices. By reducing the voltage ringing at high switching speed, this type of designs can also reduce the EMI emission from the power module.

The other benefit of using advanced packaging structure is

possibility of "double-side cooling". These structures, especially "wire-less" structures, provide two paralleled cooling paths for the SiC device from both top and bottom. This type of designs can tremendously reduce the equivalent "junction-to-ambient" thermal resistance, and thus, achieve high power density in the module.

The third benefit of using advanced packaging structure is that it is easier to achieve parasitic balancing in multiple loops while keep the same loop-minimization philosophy for each path. This advantage helps to realize multi-chip paralleled operation in SiC modules with low unbalanced in dynamic current sharing during switching transitions, and low EMI emission.

Some of the typical advanced structures are listed below.

A. Improved Wire-Bonded and Hybrid Structures

Commercial available WBG power modules employing traditional IGBT packages are mostly based on wire-bond technology and 2-Dimensional structure. Those packages, such as Econo-dual® and 62 mm packages, have high parasitic inductance (> 15 nH), and thus, to achieve stable, clean switching, the *dV/dt* of these module are usually limited to 50 V/μs. This limitation also restricts the potential of further reduction on switching losses.

The traditional wire-bonded structure has strong limitations on the parasitic control, but its advantages of maturity, simplicity and low-cost attracts the attention of manufactures.

To advance the conventional wire-bonded module design to fit with WBG device requirements while keep its advantages, lots of improvement and optimization work for wire-bonded structures has been proposed. C. Zhen from Center for Power Electronics Systems (CPES) [24] presented an improved wire-boned structure for 1200 V/60 A SiC power module in 2013 as shown in Fig. 3(a). This module adopted three-dimension (3D) leadframe in a two dimension (2D) wire-bonded multi-chip SiC module to enhance the symmetrical Kelvin Source connection for each switching device. This module also integrates the decoupling capacitors onto the substrate so that the switching ringing can be sufficiently suppressed. W. Miao and Luo. F from University of Arkansas (UARK) combined this concept with symmetrical power loop design using "double-ended-sourced" busbar structure [25] in a 15 kW SiC multichip module design as shown in Fig. 3(b), and effectively reduce the circulating current and improved the dynamic current sharing in multi-chip SiC modules. Although the external connection in these designs is 3D- leadframe, the overall module design still consists of a 2D power loop on the same single DBC plane.

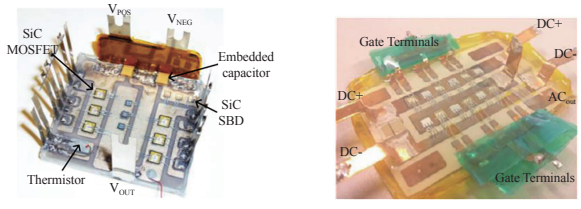


Fig. 3. Improved SiC Power Modules: (a) CPES's optimized design [24], (b) "double-ended-sourced" structure power module [25].

To further reduce the power loop inductance in wire-bonded structure, researchers started thinking of changing 2D power loop into 3D to reduce the loop area. Fig. 4 from Z. Chen and R. Wang from CPES [26], [28], and C. Chen from Huazhong University of Science & Technology (HUST) proposed a hybrid package for SiC modules [27]. This concept utilizes multi-layer substrates (DBC + DBC or DBC + PCB) to separate device die and current commutation traces, while the dies sits in a "caved space" surrounded by a second layer substrate. The top pads of devices can be wire-bonded to the adjacent trace pads on the top substrate layer, and then the current commutation will be between top and bottom substrates, therefore, the power loop current goes vertically between different layers instead of circulating in the same DBC plane.

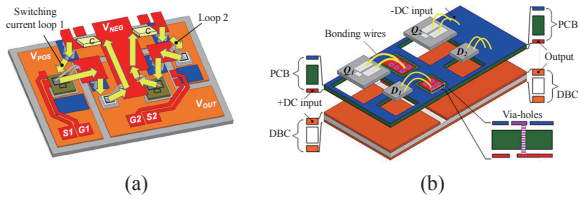


Fig. 4. Hybrid packaging structure: (a) CPES's work [26], (b) HUST's work [27].

These improved structure and hybrid structure adopts benefits from wire bonding technologies with significant reduction of parasitic inductance. The inductance of these improved structure ranges from several nH to tens of nH. However, this package still has bonding-wires, which is a major contributor to the parasitic inductances. Moreover, the use of wire-bond technology requires bonding pads on the top surface of devices. This structure limits heat dissipation from the top side of the device, which makes it hard to use "double side-cooling" concept in wire-bonded packages.

B. Wireless Structure

Wireless planar structure eliminates the bonding wires, and thus it can help to reduce the packaging parasitics. Moreover, using different bonding material with the chip upper surface, different types of planar structure can be obtained. Some of them are:

1) Direct-Lead-Bonding (DLB) Structure

A direct-lead-bonding uses a copper lead for the top side connections as illustrated in Fig. 5. The top surface (emitter/cathode) connection is made directly by Pb-free soldering of a copper tab to the chip's surface [29]. The large area of top copper

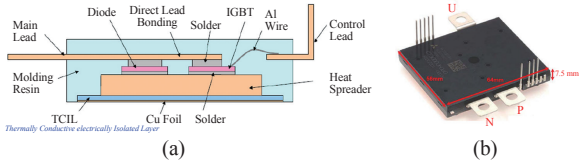
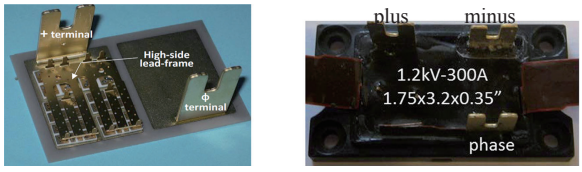


Fig. 5. Illustration of DLB technology: (a) DLB structure [29], (b) Mitsubishi T-PM DLB IGBT Module [30].

lead can form a 3D power loop to reduce the parasitics. But, the thermal performance nearly hasn't improvement. Based on this structure, the Mitsubishi had developed the T-PM DLB module (Fig. 4) [30]. Which has the internal inductance reduced to 57% and internal lead resistance reduced to 50% of a wire bonded module. Furthermore, the module has more than 10 times longer lifetime. Because of the large bonding area and less thermal expansion caused by the partial temperature dissipation on the chip surface. Although this technology has not yet been used in SiC power module, it has the potential for applying it in SiC packaging for its outstanding performances.

Based on this DLB technology, a full SiC 1200 V/300 A half-bridge module had been designed by Silicon Power Corporation [31] as shown in Fig. 6. It achieved 3x the current in 1/3 the volume of the successor commercial 1200 V/100 A PowerEx module.



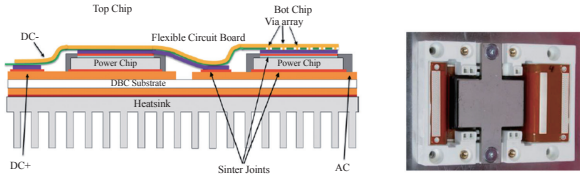
(a) (b)

Fig. 6. Full SiC DLB module by Silicon Power Corporation: (a) inside view of one segment, (b) outside view of the whole module. [31]

2) SKiN Structure

SKiN structure uses a flex printed circuit board. In which Ag sintered directly on the top of chips and the heat sink is sintered to the DBC [32]. As the loop height is reduced, parasitic inductance can be reduced up to 10% in SKiN technology. The thermal performance has no improvement. Moreover, the SKiN technology enhances the power cycling lifetime by a factor of almost 200 relatives to the classical module design and by a factor of 40 related to state-of-the-art industrial modules.

Nowadays, this technology has been further used in a 1200 V/400 A modified SiC power module design by SEMIKRON [33] as shown in Fig. 7, and a below 1 nH parasitic power module can be obtained.

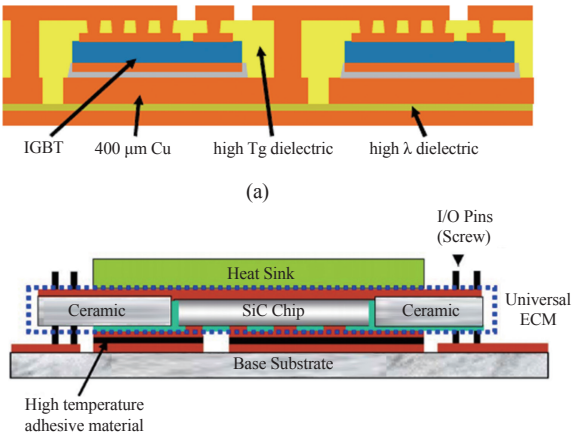


(a) (b)

Fig. 7. SKiN technology used in SiC power module: (a) Modified SKiN structure, (b) 1200 V/400 A power module. [33]

3) Embedded Structure

Embedded structure is a multi-layer design that uses a separate layer of substrate to enclose the power semiconductor devices, as shown in Fig. 8(a). In this structure, the power semiconductor devices are mounted in the openings on the ceramic frame with an adhesive polymer that surrounds the device edges or laminated PCB materials. After this assembly, Cu seed is deposited on the top as the interconnect layer for chip pad connection. And the Cu seed is filled with Cu by electroplating, and the Cu is structured by etching [34], [35]. As shown in Fig. 8(b), the sic embedded module proposed by CPES had reduced parasitic inductances, improved power density, and low mechanical stress [36]. In this structure, associated SMD components can be integrated in the module and placed on the top routing layer in this structure.



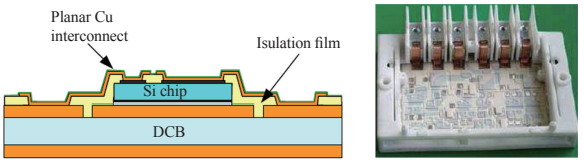
(a)

(b)

Fig. 8. Embedded structure: (a) illustration of the chip embedded [34], (b) a SiC embedded module [36].

4) Semikon Planar Interconnect Technology (SiPLIT®)

In this structure, the entire module (Fig. 9) is coated with a soft, epoxy- based insulation film applied by vacuum lamination processes. The Cu connection is developed using sputtered and galvanic Cu deposition processes (typical thicknesses are 50 μm-200 μm, depending on chip rated currents and thermal impedance requirements) [37], [38]. Since the copper connection is attached on the surfaces of DBC and chips like SKiN structure, a small loop area can be obtained. The stray inductances of this power module structure, as shown in Fig. 9(b), can be reduced by 50% (about 5 nH). A remarkable 20% R_{th}-reduction is achieved which is attributed to the additional thermal path offered by the Cu interconnects to the substrate surface. In addition, large area thermal contact improves the power cycling capability and surge current robustness significantly.



(a) (b)

Fig. 9. Illustration of SiPLIT technology: (a) cross-section of power module, (b) SiPLIT module. [37]

5) 2.5D Structure

This is also a multilayer, multi-substrate structure. The power

chips are attached on the same substrate while the other substrate is used for routing/interconnections between two power chips. The terminal pads on the power device are connected to the routing layer through metal interposers. Due to the height difference between MOSFET/IGBT and diode chips, the top side normally will add copper pin, metal post, shim material, as shown in Fig. 10 [39]-[46]. In the case that all heights of the power chips are the same, these devices can be directly attached to the top substrate. This structure had been widely used in the applications, especially the EV/HEV systems for its low parasitic and low thermal resistance features. Many SiC power modules based on this technology are also developed. Some typical modules are shown in Fig. 11. These power module [46], [47] shows beyond 30% reduction in thermal resistance and parasitic. This structure can also be considered as an "improved version" of "Press-pack" concept.

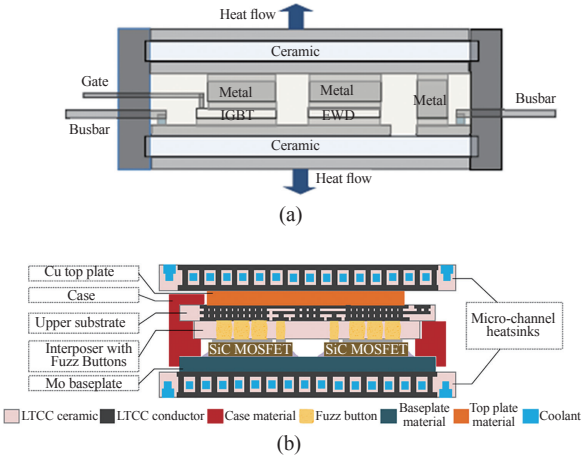


Fig. 10. Two side DBC planar bonding structures: (a) metal post connection [39], (b) pressure contact interposer connection [46].

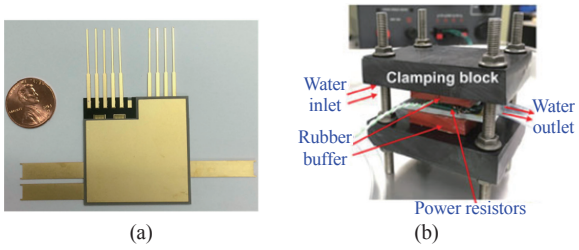


Fig. 11. Two side DBC planar bonding based SiC module: (a) ORNL's 1200 V/100 A SiC module [47], (b) uark's pressure contact interposer SiC module [46].

C. 3D Packaging Structures

3D structure can achieve extremely low parasitics (less than 1 nH), which is much lower than that in wireless structures. 3D structures discussed in this paper include power chip on chip (CoC) and wafer level CoC *etc*. 3D structure [48]-[55]. These types of structures can be summary as:

1) Chip-on-Chip (CoC) Structure

CoC is a structure that can tremendously reduce the parasitics. In this structure, two power chips are vertically conneted through a metal interconnections, such as vias, copper or solder bumps *etc*. Fig. 12 shows a press-packed chip-on-chip IGBT structure. The prototype exhibits superior switching performances with reduced parasitics and EMI emissions. Also, the CoC SiC power module can use this method. [51] proposed an only 0.25 nH ultra-low inductance embedded CoC structure design as shown in Fig. 13.

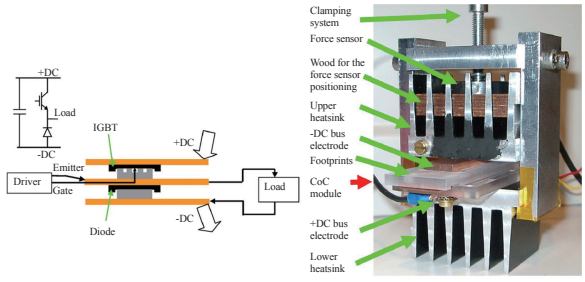


Fig. 12. Press-pack CoC IGBT buck module: (a) Electrical circuit and side view of the buck module, (b) Prototype of CoC 3D power module. [48]

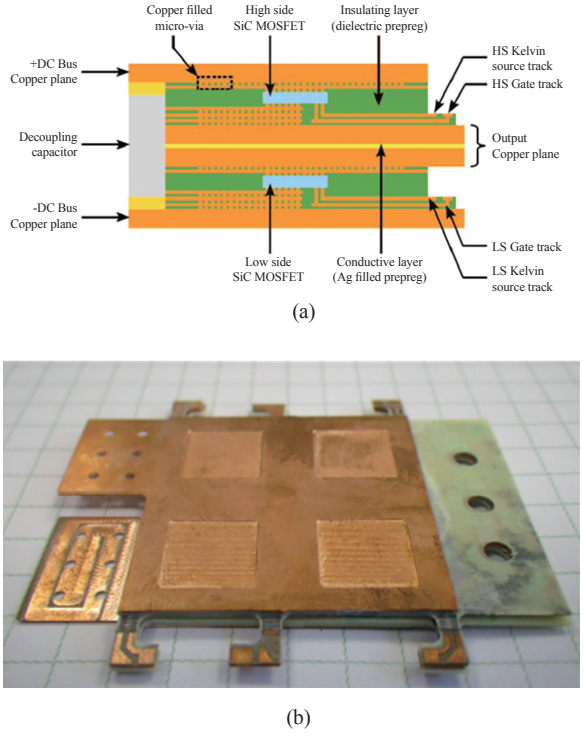
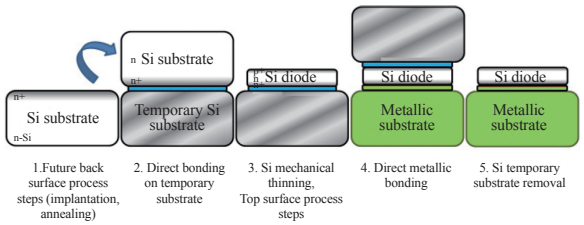


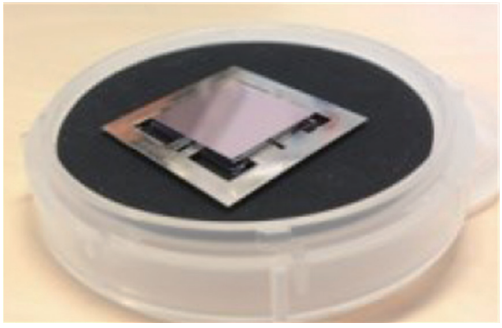
Fig. 13. CoC 3D SiC power module: (a) overview of CoC module with embedded die, (b) prototype picture. [51]

2) Wafer-Level Packaging Structure

Wafer-level chip-scale packaging technology can reduced the parasitic to smallest and especially suitable for WBG devices. Wafer-level packaging technology uses the semiconductor fabrication processes such as chemical vapor deposition (CVD), physical vapor deposition(PVD), photolithograpy and deep reactive Ion etching *etc*. to assemble devices at wafer level. Fig. 14 illustrates wafer-level copper bonding processes for the



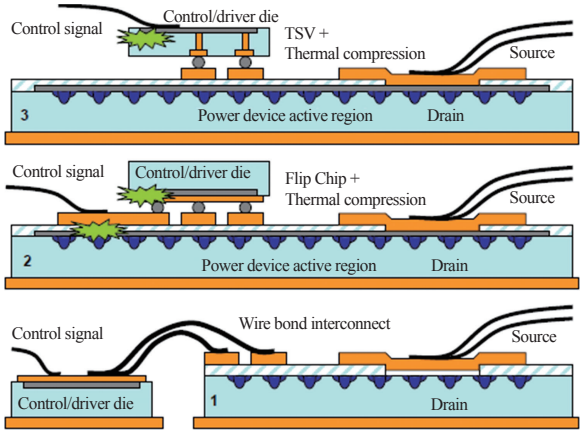
(a)



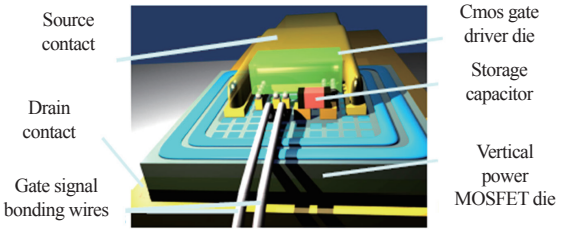
(b)

Fig. 14. 3D wafer-level packaging for vertical power devices: (a) wafer level direct bonding processes on a metallic substrate, (b) power module picture. [54]

direct attachment of high-current copper contact onto Si devices [54]. At module level, high-side and low-side power devices can be vertically interconnected through their metal contacts. Another wafer level packaging concept utilizes the Through Silicon Vias (TSVs) to connect the gate drive chips and power chips, as shown in Fig. 15 [55]. This approach provides potential solution of wafer-level integration for the gate driver and the power chip. Although these technologies had only been demonstrated in Si power module packaging, they offer attractive and inspiring features to SiC power module.



(a)



(b)

Fig. 15. Gate drive chip on power chip 3D wafer-level packaging structure: (a) TSV interconnection possibilities between the power device and gate drive, (b) Possible representation of the 3D power module. [55]

IV. Packaging Material System

The State-of-the-art silicon packaging material systems can operate up to 175ºC which is in compatible with the limits of Si devices. WBG devices, which can operate at much higher temperatures (200-350ºC) and electric fields (10x than Si devices), requires updated packaging material systems to provide compatible high breakdown voltage strength, compatible thermal-mechanical characteristics for better Coefficient of Thermal Expansion (CTE) matching with SiC material, and the capability of withstanding higher operating temperatures. These challenges mainly characterized to four parts – substrate, die attachment, bonding and encapsulation.

A. Substrate

A power packaging substrate consists of two metal layers and an insulation layer, usually a ceramic layer, in the middle. Different metal and ceramic materials provide different performances in module packaging. TABLE IV lists a comparison among four normally used ceramic materials [56]-[59]. Among all choices, Al_2O_3 is the most economic choice but has the highest thermal impedance and moderate mechanical strength. BeO has the highest thermal conductivity, however, the dust particle formed during its processing is hazardous to health. In comparison, AlN is a safe material featuring much higher thermal conductivity than Al_2O_3, and closer CTE matching with SiC materials. Its flexural strength is similar to that of Al_2O_3, so is its

TABLE IV
Main Thermal, Mechanical and Electrical Characteristics of Ceramic Substrates

	Si_3N_4	AlN	Al_2O_3	BeO
Dielectric constant	8~9	8~9	9~10	6-8
Loss factor	2×10^{-4}	3×10^{-4}	3×10^{-4}-1×10^{-3}	3×10^{-4}
Resistivity (Ω·m)	$>10^{12}$	$>10^{12}$	$>10^{12}$	$>10^{12}$
Dielectric breakdown strength (kV/mm)	10 - 25	14 - 35	10 - 35	27-31
Thermal conductivity (W/m·K)	40-90	120-180	20-30	209-330
Bending strength (MPa)	600-900	250-350	300-380	≥250
Young Module (GPa)	200-300	300-320	300-370	330-400
Fracture toughness ($MPa\cdot m^{1/2}$)	4-7	2-3	3-5	1-2.5
CTE (mm/m·K)	2.7-4.5	4.2-7	7-9	7-8.5
Available substrate technologies for thick film metallization	AMB (Cu)	DBC (Cu), AMB (Al)	DBC (Cu)	DBC (Cu)

thermal cycling lifetime. Si_3N_4 is a better choice in terms of its much higher thermal cycling reliability, but the penalties are its higher material cost and lower thermal conductivity [60].

According to the differences in manufacturing process, these substrates fall into four major categories: direct bonded copper (DBC) [61], [62], direct bonded aluminum (DBA) [63]-[66], insulated metal baseplate (IMB) [67], [68] and thick film copper (TPC) [69], [70].

1) DBC is widely used in different packaging applications because of its balance between outstanding performances and relatively low cost. DBC is made through high temperature process, during which a thin copper-oxide on the copper foil is used to create a eutectic bond between the copper and ceramic. However, the oxidization layer on the bonding interface creates a weak point of delamination, and thus, DBC has moderate life-time in thermal cycling. Active Metal Brazing (AMB) process is another choice to join the metal and the ceramic [61]. Using AMB process can eliminate the oxidization layer, and thus, it can improve the life-time of the substrate.
2) DBA has to be mentioned. [63] It uses AlSi-brazing to bond the aluminum and the ceramic. The DBA substrate with the Al alloy base plate is capable of increasing the module reliability in terms of thermal cycling. However, thermal conductivity of DBA is not better than that of DBC. To further improve the thermal conductivity of DBA substrates, lots of variations have been proposed [71]. In these variations, Al is used as a buffer to release the thermal-mechanical stresses, and a layer of copper is deployed to enhance the thermal conductivity of the substrate. Fig. 16 shows the combination of these metal layers in new DBA substrate design, which has significant increasing in life-time of their thermal cycling.

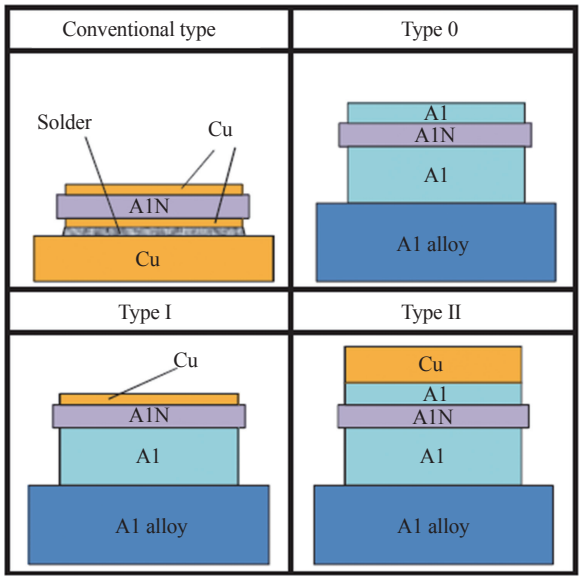


Fig. 16. Schematic showing a comparison between three types of module structures and the conventional modules structure. [71]

3) IMB is another good substrate candidate. Since IMB do not have complexity of fabrications and high temperature treatment as DBC, IMB has lower fabrication cost and long term reliability. It consists of a highly thermal-conductive insulating resin sheet, a copper baseplate and thick copper foils. IMB has good heat dissipation while satisfying the isolation requirement. It's reported in Mitsubishi IGBT module that (Fig. 17), with optimized IMB insulating material and thickness, the module's life-time in thermal cycling has been enhanced, and the effective chip-mounting area has been increased by 23% [67]. The Samsung used a similar CBM^{TM} substrate [68]. The life time reliability has been extended more compared to the DBC substrate even in extreme test conditions.

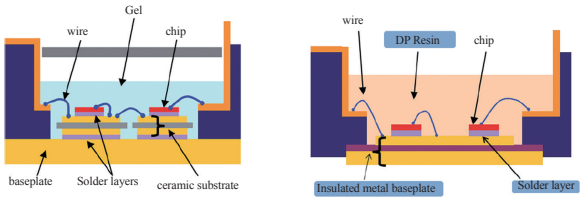


Fig. 17. Cross-sectional view of package: (a) conventional ceramic substrate and (b) proposed IMB. [67]

4) Another method to form metal bonded ceramic substrates is using TPC [69], [70] technology. Thick layers of copper paste are applied by screen printing process and are fired at 850-950 °C to sinter the metal powders and create a high adhesion bond between the metallic film and the ceramic substrate. This technology provides excellent temperature cycling reliability and opens possibility to combine power and logic components by parallel realization of thin and thick Cu pattern tracks. As shown in Fig. 18, standard DBC substrates on alumina failed before 200 thermal shock cycles (–40 °C, +150 °C), thick print copper substrates on alumina show no sign of delamination even after 2000 cycles and thick print copper on aluminum nitride remains stable up to 1800 cycles.

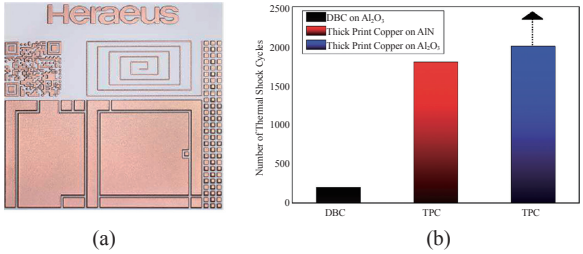


Fig. 18. TPC substrate: (a) 300μm thick printed copper substrate, (b) reliability comparison results. [69]

Fig. 19 shows the comparison of above four types of substrate, as shown in the DBA, CBM and TPC have the highest reliability. Since the constraint of high temperature isolation material for CBM, it cannot work at high temperature SiC packaging. Therefore, DBA derivative types and TPC will be a good candidate for high temperature WBG device packaging.

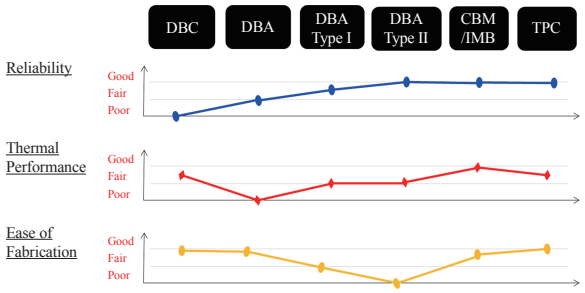


Fig. 19. Comparison of different types of substrates.

B. Die-Attaching Materials

Die-attaching materials fall into many categories, spanning both high and low temperature use. The five main categories are (1) epoxy adhesives, (2) alternative resins, (3) eutectic die attach solders, (4) soft soldering and (5) silver-glass material [72]. Two of the most commonly used die-attach materials today are solder alloys and conductive epoxy. Most silver filled epoxies used in commercial small-signal devices fail at temperatures near 200 °C. Their low operational temperatures are not workable solutions for high temperature applications. Alternative resins with the use of organic compounds are applicable also to low power Si devices.

Beyond 200 ºC, [72] had summarized the existing die attaching materials as shown in Fig. 20. In the low temperature range 200~300 ºC, the tin-lead (Pb-Sn) and lead-free tin-silver-copper (SAC) alloy solder are listed in the figure. As we can see in the middle range 300~400 ºC, the tin-lead (Sn-Pb) solder systems have high liquidus points and they have been popular for high temperature die attach materials thus far.

However, the higher the Pb content, the slower the throughput in automated die attach machines, due to the time required for the Pb-Sn liquid to re-solidify after the die attach operation is completed, causing voiding in between the die and substrates' crevice. For larger dies, which require more die attach material coverage, the voiding issue will be more pronounced. Additionally, since the ban on hazardous materials in consumer electronics since 2006, and beyond consumer electronics in the whole electronics industry nowadays, the Pb solder are forbidden [73]. Hence, the lead-free high temperature solder are emergency technology. It is worth noting that lead-free silver sintering, diffusion soldering and reactive multilayer bonding are emerging die attach technologies with the potential to provide improved chip to substrate interconnection in terms of mechanical, electrical, high temperature and thermal performance [74]-[78]. As depicted in the high temperature range in the figure, these solders have very high liquidus temperature.

Silver sintering is also known as low temperature joining technique (LTJT). The process is based on the spontaneous sinter ability of silver particles in the nano and micro scale with applied pressure at temperatures of above 220 °C [79]-[85]. Silver sintered interconnections show numerous advantages such as a remarkable high melting point of 961 °C, a far better thermal conductivity (250 W/mK) and an enhanced electrical conductivity (41 MS/m). In addition to the positive mechanical characteristics, such as a CTE value of 19 µm/mK and a good tensile strength of 55 MPa, they show considerably enhanced reliability in thermal and power cycling tests. Today, silver sin-

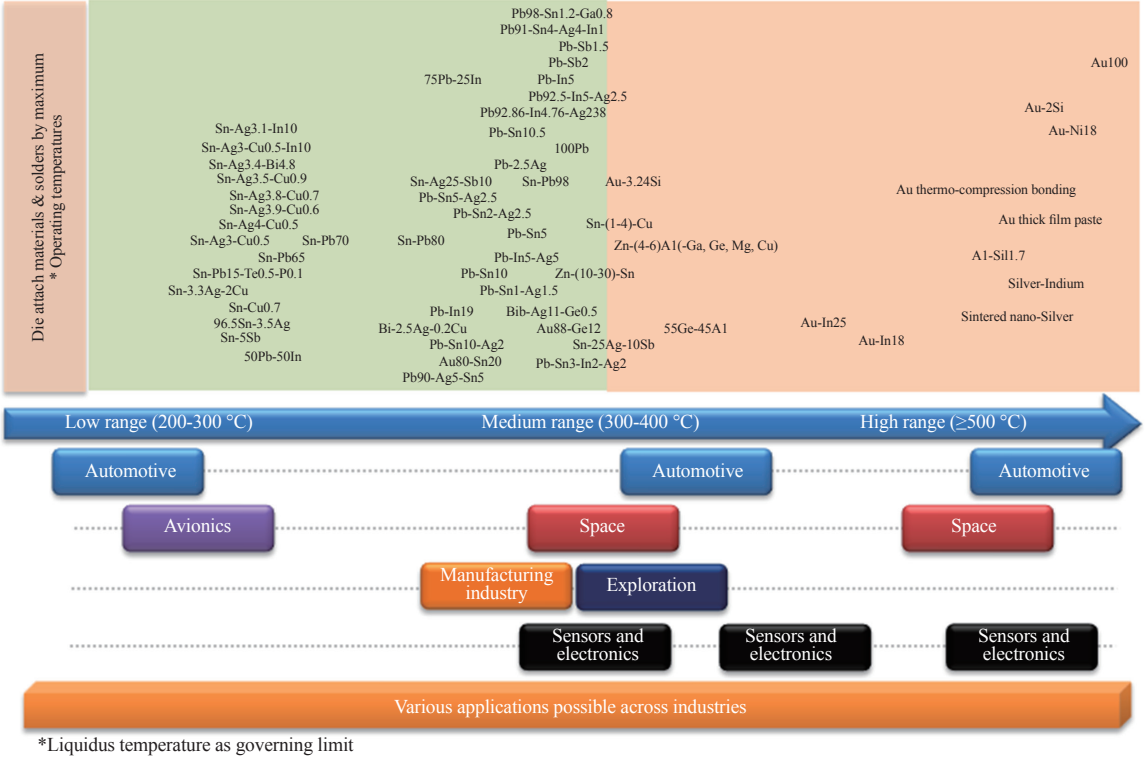


Fig. 20. Various die attach materials and solders, their operating range and application possibilities. [72]

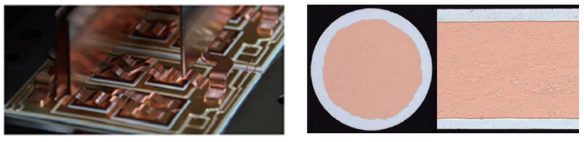
tering is applied during industrial manufacturing for a range of selected products but has not been introduced as a flexible and versatile technology platform into mass manufacturing. The root cause for the current situation is that quality issues and failures in silver-sintered contact interfaces in dependence of chip and substrate metallization, as well as variations in the sintering process, are not understood in detail and will be the aim of further research.

Diffusion soldering describes an interconnection technology based on a metal interlayer where solid-solid as well as liquid-solid diffusion between joining materials is stimulated. Transient Liquid Phase Bonding (TLPB) realized by bonding of parent materials with pre-deposited low-melting metal layer, whereas Transient Liquid Phase Soldering (TLPS) involves usage of the printed standard soft solders as interlayer for intermetallic phase (IMP) formation [77], [86]-[89]. The diffusion solder have Ag/In [90], [91], Ag/Sn [92], Au/In [93], [94], Au/Sn [95], [96], Cu/Sn [97], [98], and Ni/Sn [99]. Considered the cost and environment friendly, the Cu-Sn alloy solder has been a good candidate for high temperature applications. Because of lack of the understanding of physical principle, characterization and soldering processes, the use of these materials are not well known.

In summary, the presented new concept joining technologies show remarkable properties with the potential to improve the quality of power electronic packaging. Hence, knowledge of specific quality and reliability-affecting factors, as well as the availability of adequate testing methods for a detailed characterization of the formed metallic joints, are necessary in order to assure a high strength and a long term reliability of silver sintered, diffusion soldered or reactive bonded devices.

C. Bonding Methods

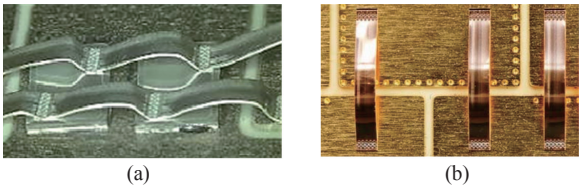
Copper wire bonding (Fig. 21(a)) is one of the most promising technologies for connecting high current interconnections in power electronics assemblies [76], [100]. The high flexibility in the layout and established quality from the aluminum wire bonding process are two reasons to promote the development of Cu wire bonding. Using copper material over aluminum for wire bond interconnections provides two key benefits such as, increase in current capacity by 37% and the excellent thermal conductivity of copper (~80% better compared to Al). Recently, novel heavy wire bonds made of an Al and Cu composite material [101] were introduced as shown in Fig. 21(b). In contrast to a pure Cu-wire no change in the metallization of the chip surface is necessary to establish a stable bonding process. The new material is still under development with the goal to increase the Cu content to a maximum without yield problems during the bonding process.



(a) (b)

Fig. 21. Novel wire-bonding: (a) Cu wire-bonding [76], (b) Cu-Al wire bonding [101].

Another bonding method should be noted is Cu and Al ribbon bonding [100], [102], [103] as shown in Fig. 22. Due to the lower number of ribbons required to achieve the same interconnect resistance as for wire bond interconnects. These connections can carry higher currents and show better power cycling capabilities in dependence of the respective bonding process and the chosen ribbon material. Al or Cu ribbon bonding is an attractive new interconnection solution for the replacement of wire bonds between the power semiconductor and the substrate.



(a) (b)

Fig. 22. Ribbon bonding: (a) Al ribbon [100], (b) Cu ribbon [102].

TABLE V
SUMMARIES CANDIDATES FOR HIGH VOLTAGE ENCAPSULATION

Material	Part Number	Manufacturer	Dielectric Constant	Breakdown strength	Temperature Range (ºC)
Dielectric Fluid	Novec® 7500	3M	5.8	35 kV, 0.1" gap	128 max.
Polyamide Imide (PAI)	Torlon® 4203	Boedeker Plastics	4.2 (@ 1 MHz)	100 – 280 kV/mm	260 max.
Epoxy	Hysol® -60NC	Henkel	21.7	550 V/mil	-
Silicone	3-6635	Dow Corning	20.5	20 kV/mm	-80 to 200
Silicone	Sylgard® 567	Dow Corning	2.79 (@ 100 kHz)	16 kV/mm	-45 to 200
Silicone	TSE3051	Momentive	2.8	18 kV/mm	-
Silicone	CF2186	Nusil	35.4	19.5 kV/ mm	-140 to 315
Silicone	R-2188	Nusil	2.6 (@ 100 kHz)	500 V/mil 19.5 kV/mm	-
Benzocyclobutene (BCB)		Dow Chemicals	2.65	530 kV/mm	

D. Encapsulation

Encapsulation materials protect the power module components from external environmental damages, such as moisture, solvents, gases, and radiations [104], [105]. In addition, encapsulation materials improve the voltage ratings of the packages, in high voltages modules (>1000 V) and prevent arcing between different electrodes. However, the soft conventional encapsulation materials mainly designed for Si conventional module are limited to low temperature of about 200 °C. Therefore, identifying new materials for higher temperature application is mandatory.

Without considering hermetic packaging where gases, vacuum and liquids can be used as dielectrics, three types of materials might be suitable for high-voltage high-temperature power electronic packaging; glasses, hydroset ceramics and polymers. The main drawbacks of glasses are they have high firing temperatures more than 500 °C and they have high Young modulus causing high thermo-mechanical stresses.

In contrast, hydroset ceramics offer low curing temperature (curing can be realized at room temperature). However, those ceramics get a high Young modulus (>100 GPa) and a coefficient of thermal expansion (CTE) between 3 and 6 ppm/°C that can induce high stresses in the structure. The CTE mismatch materials can lead to severe reliability problem.

Polymeric encapsulation is the third type of materials and can be divided into two categories: soft and hard encapsulation. Soft encapsulation materials exhibit a very low Young modulus in order of several MPa and a high CTE. Silicone gels belongs to this kind of polymers and are widely retained for encapsulating high voltage multi-chip power assemblies, due to their very high softness and high insulating electrical properties. However, the literature review shows that high temperature commercially available silicone gels exhibit a maximum temperature limit lower than 250 °C for continuous service of operation [57], [106]. The review also reveals that a trade-off between high temperature ability and softness of silicones generally exists. In fact, a slight extension of the temperature range (up to 250 °C - 275 °C) might be obtained with the use of silicone elastomers.

In the second category, polymers are relatively hard and exhibit a low CTE and a relatively high Young modulus (several GPa). The reliability of some of the second category polymers (like polyimide BPDA-PDA and PA-HT), tested at temperature exceeding the 300 °C seems satisfactory [107]. However, the deposition technique of the former and the limited thickness (50 μm) of the latter (deposited by polymer vapor deposition) reduce their use at the wafer level.

Other polymers, like benzocyclobutene BCB are candidates and are stable at the temperature above 300 °C, but the major issue encountered for thick films is the void generation during the curing process [108].

In response to the high-voltage/ high electrical-field feature in SiC modules, encapsulation material with high breakdown voltage is also important to the packaging system. Off-shelf choices for these materials include silicone Gels, PAI materials and BCB materials. TABLE V summaries candidates for high voltage encapsulation [109]-[115].

V. SiC Module Integration

SiC devices is capable of high switching speed and high-temperature operation, yet it is sensitive to the packaging parasitics. Using advanced structure can significantly help with this problem. Integrating power devices with its associate components, structurally and functionally, is another way to solve this puzzle.

Module-level integration integrates associated components, such as decoupling capacitors, gate drivers, temperature sensors, current sensors and protection circuits, in the same package. This idea has been proven to be capable of further mitigating the influences from packaging parasitics. It is a good approach to improve the density and efficiency of power electronics converters [25]-[27], [51], [116]-[123]. The Intelligence Power Module (IPM) is one of the successful products which demonstrate this concept. SiC module may require a higher level of functional and structural integration trimmed for the new characteristics of the device [27], [51], [53], [55], [121], [122], [124].

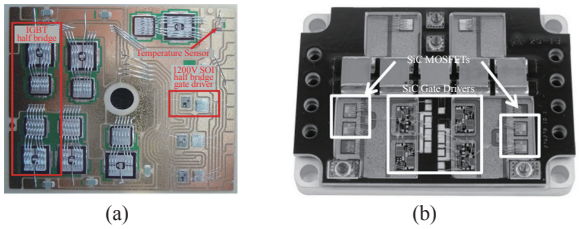
A. Integration of Decoupling Capacitor

References [24]-[28], [51] described a solution that embedded discrete Multilayer Ceramic Capacitor (MLCC) decoupling capacitors in the SiC modules, as shown in Fig. 13. This integration approach can significantly reduce the distance between power device pair and the decoupling capacitors, and thus reduces power loop parasitics, suppresses the voltage overshoot and improves current sharing among paralleled devices. This method can achieve clean switching waveforms, low electromagnetic interference, and higher power efficiency at high switching speed.

B. Integration of Gate Driver

Integrating gate drives with the power chip in the module can tremendously reduce the gate driving loop inductance and improve the driving performances. Using Silicon-on-Insulator (SOI) technology or SiC low voltage device technology, high-temperature gate driver integration can be realized in SiC modules.

Fig. 23 illustrates an integrated design from SEMIKON that SOI gate driver ICs is directly mounted on the DBC substrate in



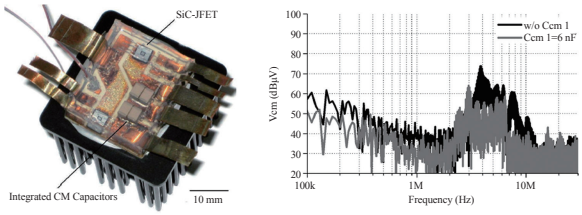
(a) (b)

Fig. 23. Integration of decoupling capacitor and gate driver: (a) SOI gate driver integration in IGBT power module [126], (b) decoupling capacitor and SOI gate driver integration in SiC power module [119].

a 1200 V IGBT half-bridge MiniSKiiP module [125], [126] and demonstrated significant improvement in the module switching performance. The University of Arkansas had developed a SiC half-bridge switching module with integrated SiC gate drivers and dc-decoupling capacitors [119], [127]. The integrated gate drivers require no gate-damping resistance because of the extrememly low parasitic gate inductance.

C. Integration of EMI Filters

Increasing switching speed is usually an advantage from the thermal and efficiency points of view, yet it has detrimental effects on the EMI emission. The "side-effects" of fast switching is that SiC module may generate too much EMI noises, and thus, a more bulky EMI filter is required at the converter level. Integrating EMI filters in SiC module and "self-containing" the noises within the module is a promising approach from converter design point of view. References [123], [128] provide a solution to directly integrate the CM filter capacitors in the power module, as shown in Fig. 24. This makes it possible to "capture" the high-frequency harmonics directly at the source.



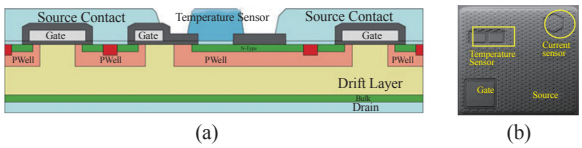
(a) (b)

Fig. 24. The power module with integrated common mode filtering: (a) SiC-JFET power module prototype with integrated CM capacitors, (b) EMI spectrum comparison between with and without integration. [123]

D. Integration of Sensor

Integrated sensors are often present in Si- IGBTs [129] or power modules like in Infineon's MIPAQ family, providing valuable information, which can be used either for monitoring, failure mitigation or studying the device aging. It is then obvious that such information is valuable for SiC-MOSFETs as they begin to be integrated into power systems.

Temperature and current sensors can be integrated into the package separated from the main device; in this case, providing information on the package temperature and device current. However, this type of method cannot react fast and the additional current sensor will increase the loop distance. The sensor integrated in the SiC-MOSFET active area by monolithic integration technology will be an emerging technology to solve it. This can provide a more precise temperature measurement in the device itself, allowing fast reaction in case of failure and more accurate information. As shown in Fig. 25, [124] proposed a SiC MOSFET with monolithic integrated sensor.

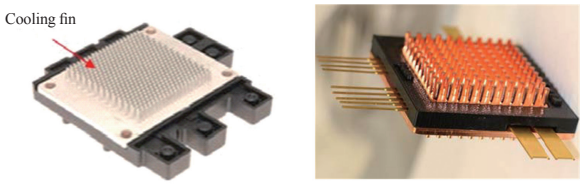


(a) (b)

Fig. 25. Monolithic integrated sensor in SiC MOSFET: (a) schematic of cross-section, (b) SEM picture of fabricated 2.25 mm^2 SiC power MOSFET with monolithically integrated temperature and current sensors. [124]

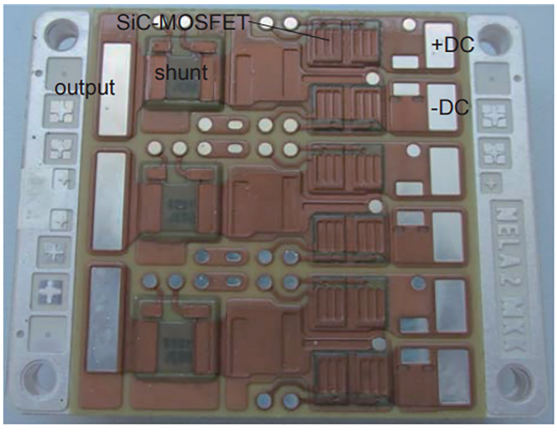
E. Integration of Thermal Management System

In a SiC power module, the heat-sink can be integrated with the baseplate or with the DBC. This integration strcture can significantly reduce the thermal impedance in the module through eleminating thermal-interfaces between the SiC device die and the ambient. Nowadays, the pin-fin baseplate power module [130]-[133] is widely used in automotive applications. The power module described in reference [130]-[133] integrated pin-fin on the baseplate and can be directly mounted on a liquid cold plate. Fig. 26(a) shows the new Mitsubishi J1-Series pin-fin integrated IGBT module, which demostrate a 76% weight reduction and 30% thermal performance improvement for three phase inverter solutions. Fig. 26(b) shows a pin-fin integrated, double-sided cooled, SiC module design from ORNL [47] , which achieves a 40% reduction in thermal resistance.



(a) (b)

Fig. 26 Pin-fin integrated power module: (a) Mitsubishi J1-Series IGBT module [130], (b) SiC pin-fin double sided cooling module [47].



(a)

(b)

Fig. 27. Full SiC power module with cooling sintering on substrate: (a) top view, (b) side view. [134]

However, the mechanical assembly and the liquid sealing for the pin-fin module is a weak point in the system, and a threaten to the life-time of the module. An alternative approach is to sinter the ceramic substrate directly onto a sealing-free heatsink such as a microchannel copper cooler [134]. This combination offers a very low thermal path between substrate and cooling liquid. Fig. 27 shows a SiC power module [134] with ceramic substrate directly sintering on a sealing-free heatsink micro-channel copper cooler.

VI. Conclusion

This paper provides overview for the state-of-the-art packaging technologies for SiC power modules. The paper covers the information regarding off-shelf SiC devices and the advanced packaging technologies from on-going research efforts. The paper summarizes these research advancements for SiC modules from three aspects: (1) module layout and structures, (2) new packaging material systems, and (3) module integration trend.

According to existing literatures, the focal points of on-going SiC module research include: (a) parasitic inductance minimization for power loop and gate loop, (b) high temperature operation design and (c) module integration to further optimize SiC switching operation with EMI noises self-containment and better thermal management. Most of the new packaging layouts, structures and integration schemes are developed for reducing the influences from package parasitics and side-effects of fast switching. The packaging materials system for SiC device is more determined by its nature of high temperature/high electric-field operation. The design trade-off is typically in thermal-mechanical-electrical multi-physics domain. Integration is an important trend for SiC devices as it provides numerous benefits for SiC switching operation. All these new approaches are for the purpose of unleashing the intrinsic benefits from SiC devices in its applications to achieve higher power density and efficiency over Si-based power conversion. It is clear that, duplicating Si packaging technologies and "dropping-in" SiC device will not have desire performance output that matches to SiC characteristics. New packaging architecture trimmed for SiC is required for future power electronics systems.

Thermal management is another important topic for SiC packaging, yet its content is relatively independent to the device itself and worth another paper dedicate on this topic.

Acknowledgment

The authors would like to express their appreciations to Mr. Amol Deshpande and Mr.Yingzhuo Chen for their helps in collecting literatures in related areas.

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Review of GaN Totem-Pole Bridgeless PFC

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***Abstract*—Switching-mode AC/DC converters are widely used in modern power supplies for computers, data centers and telecommunication equipment. Achieving Power Factor Correction (PFC) and high efficiency are the two most important requirements. In many cases, high power density is also of tremendous interest. Both power efficiency and power density are greatly influenced by the power devices, the topology and the control used. Compared with conventional Si power MOSFET and Si super-junction MOSFET, the newly introduced 600 V GaN devices not only eliminate the reverser recovery, but also have much lower switching and driving losses. These excellent properties enable the emergence of the totem-pole bridgeless AC/DC converter as the next generation preferred solution for PFC instead of the state-of-the art Si-based boost PFC. In this paper, the key technologies and designs for both hard-switching and soft-switching GaN totem-pole PFC are reviewed and the key performance metrics are compared. A soft switching, 3.2 kW totem-pole PFC prototype with 99% efficiency and 130 W/inch3 power density has been achieved in the author's group as a proof of the concept. Based on the power density comparison, the high frequency soft-switching GaN totem-pole PFC is the preferred choice to achieve both high efficiency and high power density at the same time.**

***Index Terms*—Bridgeless PFC, PFC, soft switching, totem-pole PFC, WBG power device.**

I. Introduction

SWITCHING-MODE AC/DC converters are widely used in modern power supplies for computers, data centers and telecommunication equipment [1]. It is predicted that the data center alone will consume about 10% of the total electricity by 2020 [1]. High efficiency and high power density are two factors driving the technology innovation and evolution.

Before the emerging of the wide-band-gap (WBG) devices, the 600 V Si super-junction (SJ) MOSFETs are the-state-of-the-art power devices for offline AC/DC power supplies with a 400 V DC bus and with a power level below several kW. Due to the poor reverse recovery property of the Si MOSFET and Si SJ MOSFETs, negative current condition is not preferred in these devices and it is hard to find a topology better than the conventional Boost power factor corrector (PFC) operating in Continuous Conduction Mode (CCM). The semi-bridgeless dual-Boost PFC has lower conduction loss, but its utilizations of the devices and the inductors are much worse compared with the conventional Boost PFC [2]. Thus, in the past few decades, the conventional Boost PFC has been the most mature solution for the single phase offline PFC. Due to the relatively large switching loss, the switching frequency is typically below 100 kHz, limiting the reduction of the converter size. Two example of hardware based on the conventional Boost PFC with Si SJ MOSFETs are shown in Fig. 1 [3], [4].

(a) (b)

Fig. 1. Examples of hardwares based on the conventional Boost PFC with Si SJ MOSFETs: (a) Eltek product AC/DC (PFC+LLC) product, 3 kW, 4.25 x 1.69 x 13 inch^3 [3]; (b) ST 3 kW PFC evaluation board, 9.6 x 4.3 x 1.4 inch^3 [4].

The emerging of the 600 V GaN devices, which have low on-resistance, fast switching speed, and zero reverse recovery loss, are fundamentally changing the above conclusion hence the design of the AC/DC converters [5], [6]. For the PFC stage of the AC/DC power supplies, the totem-pole bridgeless PFC with 600 V GaN devices has shown superior performance compared with the conventional Boost PFC and the semi-bridgeless dual-Boost PFC [1], [7]. The GaN totem-pole PFC can achieve very low conduction loss thanks to the ever decreasing device R_{on} that is inherently a feature of any WBG power device [5]. The device and inductor utilization is high and the EMI noise is also low in the totem-pole PFC [7]. The GaN totem-pole PFC can work under hard-switching mode or soft-switching mode. Note that, for hard-switching mode, the totem-pole PFC cannot be used with the Si SJ MOSFETs due to the severe reverse recovery loss in SJ MOSFETs. However, the GaN totem-pole PFC has been proven to be able to work under hard-switching mode with 99% efficiency due to the elimination of the reverse recovery issue [7], [9], [10]. In the hard switching case, the dominant dynamic loss is the device's turn-on loss since the turn off loss is very low due to the lossless charging of the output capacitance C_{oss} of the device [5], [6]. The dominant turn-on loss can be further eliminated by employing the zero-voltage-switching (ZVS) technique in which the energy stored in the output capacitance E_{oss}, is recovered. ZVS based GaN totem-pole PFC has been shown to operate well above 1 MHz switching frequency while still maintain 99% efficiency [1], [8]. The soft-switching GaN totem-pole PFC with increased switching frequency and efficiency therefore significantly improves the power density compared with the CCM Boost PFC [1], [8].

This paper is organized as follows. In Section II, the 600 V GaN devices are discussed in detail. In Section III, the topologies of GaN totem-pole PFC is reviewed and compared with the con-

Manuscript received August 24, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00018

ventional PFC topologies. In Section IV and V, the technologies and the performances of the hard-switching and soft-switching GaN totem-pole PFC are reviewed respectively. Finally, the summary and conclusions are included in Section VI.

II. 600 V GaN FETs

GaN heterojunction FET (HFET) is a superior device that is commercially available from 30 V to 600 V. The device is typically fabricated on GaN-on-Si wafers and utilizes a lateral structure with Source, Gate and Drain terminals all on the same side of the wafer. A lateral structure has lower utilization of the chip area compared with a vertical power device. However, this is not a major factor preventing the GaN HFET to achieve amazing performance gains over competing vertical Si power devices such as Si SJ MOSFET. Due to the high channel mobility (~2000 cm^2/V-s) and the elimination of the substrate conduction resistance R_{sub}, as well as the very short drain to source spacing requirement that is inversely proportional to the peak electric field strength of the GaN material, the lateral GaN HFET's R_{on} is still significantly reduced for a given chip size. This reduction in R_{on} or $R_{on\text{-}sp}$, directly results in the reduction of the chip size which translates to smaller device capacitance. Furthermore, the lateral HFET structure where the charge layer is concentrated on a thin top layer and the terminals are non-overlapping with each other, the junction capacitance (C_{iss}, C_{oss}) is further reduced compared with vertical devices even if the chip area is the same. Thus, the smaller chip size and the lateral structure both contribute to a substantial reduction of the device capacitance. This feature makes the GaN HFETs very close to an ideal high frequency switch. Due to the absence of any PN junction in the GaN FET, there is no minority carrier injection hence no stored charge. This results in a reverse recover free operation of the GaN HFET when it is used as a rectifier. This is a major advantage of GaN over Si power MOSFETs.

The performances of the 600 V state-of-the-art Si SJ MOSFET, SiC MOSFET and GaN HFETs are compared in TABLE I. Three normalized device figure of merits (FOMs) are comapred in TABLE I. The smaller the FOM, the better the device is. FOM1 represents the speed of the gate driving. The smaller the FOM1, the faster the gate drives. For FOM1, both SiC and GaN devices are much better than Si SJ MOSFET. The enhancement-mode GaN FETs have much smaller FOM1 than SiC MOSFET. However, the SiC MOSFET has smaller FOM1 than cascade GaN FET. This is caused by the high input capacitance of the integrated low voltage Si MOSFET in the cascode GaN structure. FOM2 represents the switching loss for both hard-switching and soft-switching. The smaller the FOM2, the less the switching loss. Note that the state-of-the-art Si SJ MOSFET of Infineon G7 series has even lower FOM2 than SiC and GaN devices. And GaN FETs are not better than SiC MOSFETs. FOM3 represents the reverse recovery loss. The smaller the FOM3, the less the reverse recovery loss. Both SiC and GaN devices have significant reduction of the reverse recovery loss. The enhancement-mode GaN FETs have zero reverse recovery loss. The reverse recovery loss of the cascode GaN FET is not zero due to the reverse recovery loss of the low voltage Si MOSFET. The severe reverse recovery loss of the Si SJ MOSFETs causes that the synchronous rectification of Si SJ MOSFETs is not preferred under the hard switching condition. However, the WBG devices have changed this phenomenon, especially the enhancement-mode GaN devices, since they eliminate the reverse recovery issue. This in turn enable the use of totem-pole circuit for PFC as discussed in the next section.

TABLE I
COMPARISON OF 600 V FETS

600V FETs	Part Number	R_{on} (mΩ)	C_{iss} (nF)	FOM1 (R_{on}•C_{iss})	Q_{oss} (μC)	FOM2 (R_{on}•Q_{oss})	Q_{rr} (μC)	FOM3 (R_{on}•Q_{rr})
Si SJ	IPT60R028G7 [11]	28	4.82	135	0.074	2.072	8.7 (100A/μs, 400V)	243.6
SiC MOS	SCT3030 [12]	30	1.53	45.9	0.085	2.55	0.13 (1100A/μs, 600V)	3.9
Enhancement-Mode GaN FET	GS66516T [13]	25	0.52	13	0.113	3.25	0	0
	PGA26E07BA [14]	56	0.405	22.68	0.045	2.52	0	0
Cascode GaN FET	TPH3207WS [15]	35	2.2	77	0.11	3.85	0.18 (1000A/μs, 400V)	6.125

III. Topology of GaN Totem-Pole Bridge-Less PFC

The Boost PFC is the most conventional topology for the server power supply products [2]-[4], [16]-[19]. As shown in Fig. 2(a), a diode bridge rectifier is cascaded with a Boost converter. A diode with low reverse recovery charge has to be used. A popular choice is to use a 600 V reverse-recovery-free SiC Schottky diode. The Boost PFC has low cost, low CM noise and high reliability. However, the efficiency is low due to the high conduction loss in the diodes.

The semi-bridgeless dual-Boost PFC, as shown in Fig. 2(b), eliminates one low frequency diode in the line current path [20]-[22]. Thus, the efficiency is improved compared with the conventional Boost PFC. Since the grid side is directly connected to the DC side by D_1 or D_2, the common mode (CM) noise is also low. In this topology, the two Boost converters will alternatively work during the positive and negative half line cycles. The low utilization of the inductors and devices reduces the power density and increases the cost compared to the conventional Boost

PFC.

The totem-pole bridgeless PFC, as shown in Fig. 2(c), has only one MOSFET and one low frequency diode conducting at any time. Thus, it has the lowest conduction loss compared with the conventional Boost PFC and the semi-bridgeless dual-Boost PFC [2], [23]-[26]. This topology consists of one high-frequency half-bridge (S_1 and S_2) and one line-frequency half-bridge (D_1 and D_2). During the positive half line cycle, since D_2 is conducted, the grid neutral point is connected to the negative terminal of the DC side. S_2 is the active switch, while S_1 acts as the synchronous rectifier (SR) switch. During the negative half line cycle, since D_1 is conducted, the grid neutral point is connected to the positive terminal of the DC side. S_1 is the active switch, while S_2 is the SR switch. In the totem-pole PFC topology, the body-diode of S_1 or S_2 provides the freewheeling path of the inductor current. Thus, if the Si SJ MOSFETs are utilized for S_1 and S_2, the totem-pole PFC cannot work at hard-switching mode due to the extremely severe reverse recovery issue of the Si SJ MOSFETs as clearly shown in TABLE I. Therefore, with Si SJ MOSFETs, the totem-pole PFC has to operate in soft-switching mode, such as the critical conduction mode (CRM) or the quasi-square-wave (QSW) mode [24]. However, with Si SJ MOSFETs, even a single hard switching event would possibly destroy the device due to the large reverse recovery energy and voltage over-shoot. Hence ensuring the soft-switching in Si based totem-pole is needed and this drives up the cost and system control complexity. Thus, even though the totem-pole bridgeless PFC has been proposed for more than twenty years, it does not receive much attention until the emerging of the 600 V GaN devices.

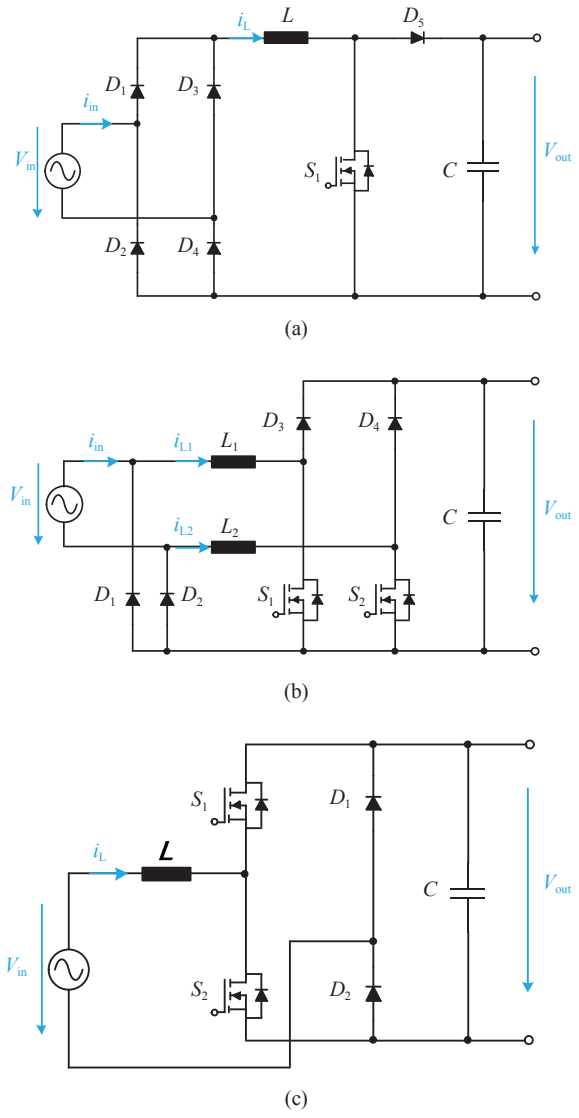


Fig. 2. (a) conventional Boost PFC; (b) semi-bridgeless dual-Boost PFC; (c) conventional totem-pole bridgeless PFC.

As discussed in the previous section, the 600 V GaN FETs not only eliminate the reverse recovery issue, but also achieves low switching loss. Thus, the GaN totem-pole bridgeless PFC, as shown in Fig. 3, draws tremendous interests from industry and academia. Compared with the conventional totem-pole bridgeless PFC, Si SJ MOSFETs are replaced by GaN FETs for S_1 and S_2. Since there is no reverse recovery issue, the GaN totem-pole can work at either hard-switching or soft-switching mode. For soft-switching mode, even if several switching cycles lose the soft-switching, the GaN FETs would not be destroyed. Hence the reliability of the soft-switching GaN converter is still high. In addition, the two low frequency diodes are further replaced by two line-frequency Si SJ MOSFETs to take advantage of their low condition loss once they are turned on. As shown in Fig. 4, during the positive half line cycle, S_4 is reversely conducting the AC grid current since the neutral point is connected to the negative terminal of the DC side. During the negative half line cycle, S_3 is reversely conducting the grid current by connecting the grid neutral point to the positive terminal of the DC side. Thus, there are no diodes in the line current

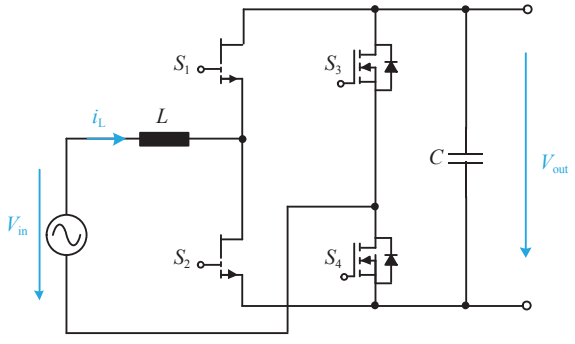


Fig. 3. GaN totem-pole bridgeless PFC.

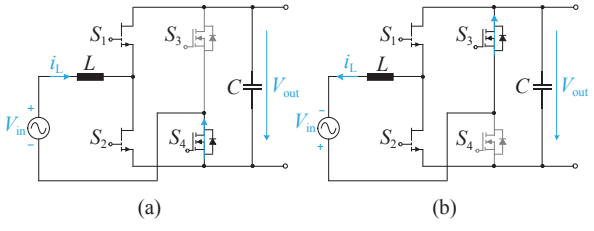


Fig. 4. Equivalent circuit during (a) positive half line cycle, and (b) negative half line cycle.

path. The GaN totem-pole PFC therefore could realize the lowest conduction loss compared with the conventional Boost PFC, the semi-bridgeless dual-Boost PFC and the conventional totem-pole PFC. Moreover, since the inductor and the GaN FETs are fully utilized in both positive and negative half line cycles, the power density also can be improved.

IV. Hard-Switching Totem-Pole PFC

The hard-switching totem-pole PFC utilizes the constant frequency pulse width modulation (PWM). Thus, hardware design and controller development for the hard-switching totem-pole PFC is as simple as those for the hard-switching conventional Boost PFC.

A. Control

With constant frequency CCM operation, the inductor current for the positive half line cycle is shown in Fig. 5.

The simplified control diagram is shown in Fig. 6 [7], [27]. The outer loop is the low-bandwidth DC voltage loop. The output of the voltage controller is the amplitude of the current reference. The inductor current is sensed and filtered. The output of the current controller is the duty-cycle. Then, the constant frequency PWM and the AC voltage polarity together determine the gating signals of G_1 and G_2. The gating signals of G_3 and G_4 are only determined by the AC voltage polarity.

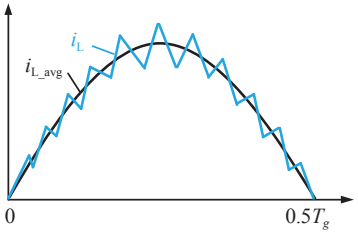


Fig. 5. Inductor current waveforms of hard-swicthing GaN totem-pole PFC.

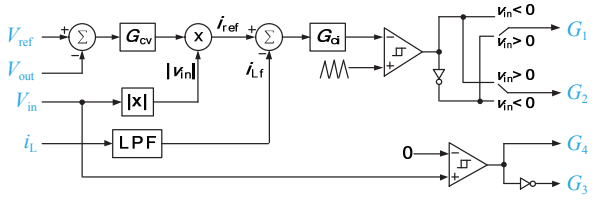


Fig. 6. Control diagram of hard-switching GaN based totem-pole PFC.

B. Frequency and Magnetic

Even though the turn on losses of the GaN FETs are much lower than those of the Si SJ MOSFETs, the turn on loss is still one of the dominated parts in the total power loss of the hard-switching totem-pole PFC. To achieve 99% efficiency, the switching frequency must be kept low such as 100 kHz which is very similar to the frequency of the hard-switching Boost PFC. Thus, the sizes of the switching frequency related passive components, including the EMI filters and the main inductors, are not improved. The total power density of the hard-switching GaN totem-pole PFC is still limited, even if the efficiency can be up to 99%.

An inductor for a 3 kW 100 kHz hard-switching GaN totem-pole PFC is shown in Fig. 7. The size is 50x40x51 mm^3. Actually, the CCM GaN totem-pole PFC can use the same inductors as the CCM Boost PFC under the same power and frequency conditions.

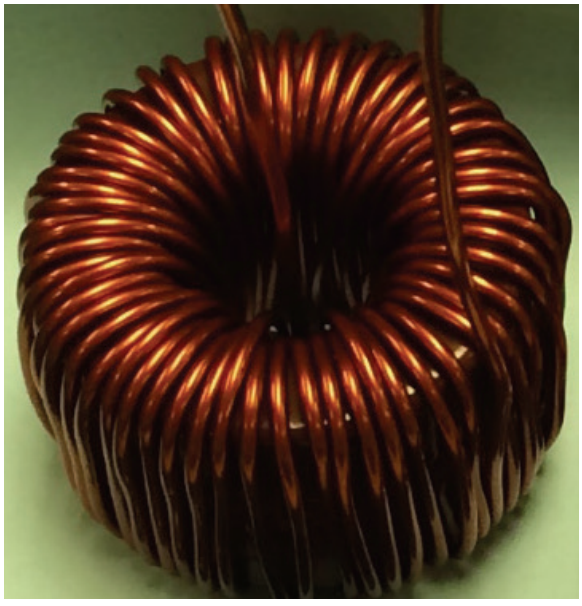


Fig. 7. An inducor (size: 50x40x51 mm^3) for a 3 kW 100 kHz hard-switching GaN totem-pole PFC.

C. Efficiency and Density

Two examples of the hard-switching GaN totem-pole PFC are shown in Fig. 8 [29], [27]. Both of them are working at about 65 kHz, and have 99% peak efficiency. A detailed com-parison of the hard-switching PFC is listed in TABLE II. Compared with the-state-of-the-art Boost PFC and the Semi-bridgeless PFC, GaN totem-pole PFC has higher efficiency. However, since the frequency is not increased, the hard-switching GaN totem-pole PFC does not improve the power density. The state-of-art CCM GaN totem-pole PFC prototypes only achieve lower than 70 W/inch^3 power density [27]-[29].

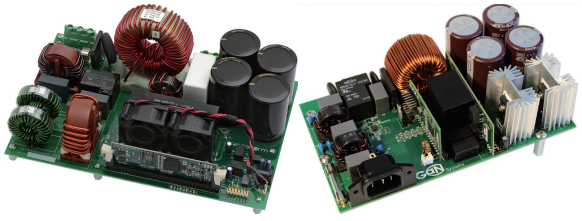


Fig. 8. Examples of hard-switching GaN totem-pole PFC: (a) Transphorm 4 kW, 66 kHz [29]; (b) GaN Systems 3 kW, 65 kHz [27].

TABLE II
COMPARISON OF HARD-SWITCHING PFC

Topology	Company	Power (kW)	Switching Frequency (kHz)	Efficiency of half load (%)	Efficiency of full load (%)	Power Density (W/inch^3)
Boost PFC	ST [4]	3	111 (3 channels)	98.7	98.5	52
Semi-briddge-less PFC	Infineon [30]	3	90	98.6	98.2	<70
	Infineon [28]	2.5	65	99.1	98.6	<70
GaN totem-pole PFC	GaN Systems [27]	3	65	99	98.7	<70
	Transphorm [29]	4	66	99	98.5	<70

V. SOFT SWITCHING TOTEM-POLE PFC

As discussed previously, increasing the switching frequency is the most straightforward way to improve the power density of the totem-pole PFC. However, the switching loss is still a big barrier. Since the turn off losses of GaN devices are less than one tenth of the turn on losses, zero-voltage-switching is potentially a great way to increase the switching frequency and keep a high efficiency. The turn-off loss can approach zero if hard-driven gate is utilized [1], [5], [6], [9].

A. Dual-Mode Soft-Switching Operation

For conventional Boost PFC, critical conduction mode (CRM) can be used to achieve ZVS soft-switching [31], [32]. How-ever, when the input voltage is lower than half of the output voltage, only partial ZVS can be achieved [32]. For totem-pole PFC, since there are two high-frequency switches in one half bridge, quasi-square-wave (QSW) mode can be utilized to achieve fully ZVS under any voltage ratios [8], [33]-[35]. Thus, a dual-mode soft-switching operation is proposed in [33]-[35].

As shown in Fig. 9, there are two operation modes during one half line cycle. When the input voltage is lower than half of the output voltage, the converter operates in CRM. In CRM, the SR GaN FET is turned off when the inductor current becomes zero. The drain to source voltage of the active GaN FET is resonant from V_{out} to zero. Thus, ZVS can be realized. When the input voltage is higher than half of the output voltage, the converter operates in QSW mode. In QSW mode, the SR GaN FET is turned off when the inductor goes down across zero and to the required negative current. The negative inductor current provides additional energy to help discharge the output capacitances (C_{oss}) of the GaN FETs and the parasitic capacitance of the inductor.

In CRM, the SR turn off current i_{SR_off} is zero. In QSW mode, the required SR turn off current i_{SR_off} decreases with the increasing of vin. i_{SR_off} can be calculated by the sensed signals (v_{in} and V_{out}) and the circuit's parameters (L and C_{oss}) [33]-[35]. This dual-mode soft-switching operation not only achieves full-range ZVS, but also minimizes the conduction loss under full-range ZVS.

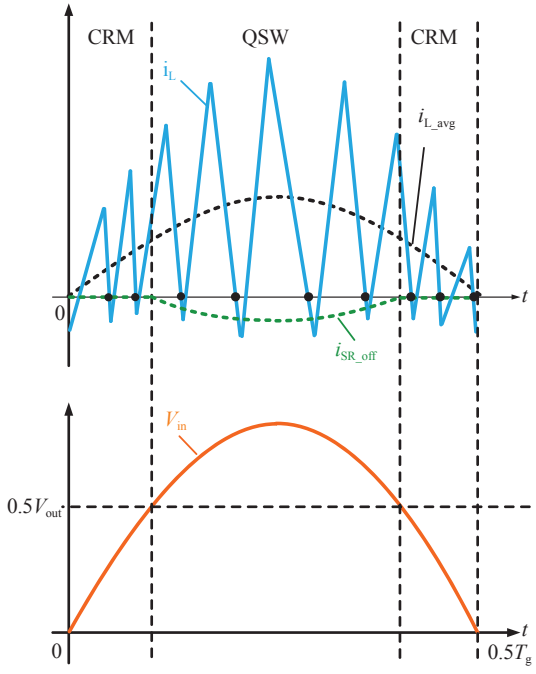


Fig. 9. Inductor current waveforms of soft-swicthing GaN totem-pole PFC.

B. Control

Two control methods can be used for the soft-switching totem-pole PFC. One is the hysteresis current control [36]. Upper and lower current reference bands determine the on/off of the switches. However, high-speed and isolated inductor current sensing is very challenging. Another control method is the on-time control as shown in Fig. 10 [33]-[35]. A zero-crossing-detection (ZCD) is needed to generate the ZCD signal. With the

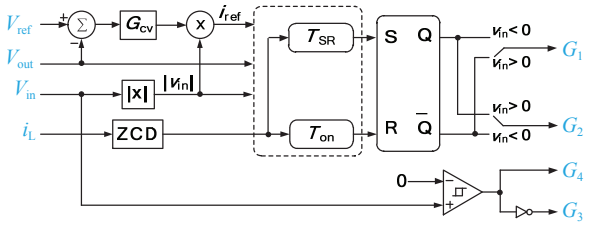


Fig. 10. Control diagram of soft-switching GaN based totem-pole PFC.

ZCD signal, gating signals are determined by the calculated active-GaN-FET on time and SR-GaN-FET on time.

The conventional ZCD method uses the current shunt, the high-speed comparator and the digital isolator to generate and transfer the ZCD signal [33]. However, this method not only causes additional loss on the current shunt, but is also sensitive to the noise. Paper [37] proposes an advanced method which uses the saturated inductor and the comparator to generate the ZCD signal. This method not only reduces the loss and cost, but also improves the noise-sensitivity.

C. Frequency Range and Magnetics

The frequency variation for the dual-mode soft-switching totem-pole PFC is shown in Fig. 11. Due to the need to achieve the ZVS, the frequency is varying and can be much higher than the hard-switching totem-pole PFC. The frequency can be from several hundred kHz to several MHz [33]-[35].

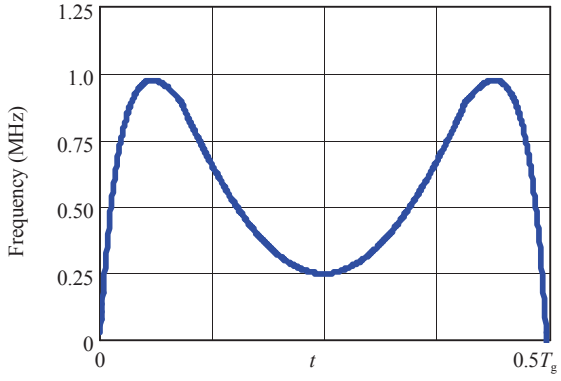


Fig. 11. Switching frequency variation under the conditions: P_{out}=1.6 kW, v_{in}=240 VAC, V_{out}=400 V, L=9.5 μH.

The high frequency inductor design is a challenge for soft switching totem pole PFC. Four high frequency ferrite materials are compared under 100 °C and 1 MHz as shown in Fig. 12 [38]-[41]. The four materials are 3F45 of FERROX-CUBE, N49 of TDK, P61 of ACME, ML91S of HITACHI. The core loss data under sinusoidal excitation without DC bias obtained from the datasheets are shown in Fig. 12(a). However, in totem-pole PFC, the inductors are usually under rectangular excitations. The core loss data under rectangular excitations without DC bias, which can be obtained by testing [42], [43] or calculations [44], are shown in Fig. 12(b). By comparing Fig. 12(a) and (b), significant difference is observed. For the same material, the core loss under rectangular excitation is much higher than the core loss under sinusoidal excitation. In addition, under sinusoidal excitation, the core loss of P61 is similar to that of ML91S. However, under rectangular excitation, the core loss of ML91S is much less than that of P61. In general, ML91S from HITACHI is the best among the four materials.

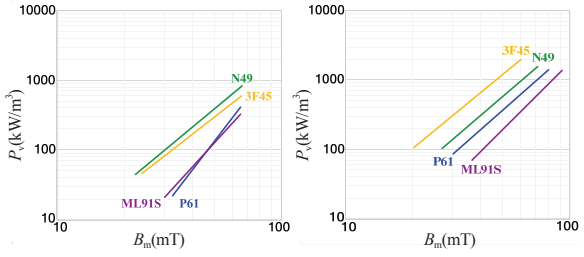


Fig. 12. Core loss of four materials under 100 °C and 1 MHz: (a) sinusodial excitation without DC bias; (b) rectangular excitation without DC bias [38]-[41].

The ferrite core shapes are also critical for the high-efficiency and high-density inductor design. Based on the data in Fig. 12, the core loss significantly increases as the flux density swing ΔB increases. ΔB is formulated as

$$\Delta B = \frac{E\Delta t}{NA_e} \tag{1}$$

where $E\Delta t$ is the voltage-second of the inductor, N is the number of turns, and A_e is the effective area. Thus, increasing N or A_e can reduce ΔB. However, increasing N will significantly increase the winding loss. This is not only caused by the need for more windings, but also by the increasing of the gap length which leads to the fringing effect. The calculation of the gap length l_g is derived as

$$l_g = \mu_0 N^2 \frac{A_e}{L} \tag{2}$$

where μ_0 is the permeability of the air. l_g is proportional to N^2 and A_e. Thus, increasing A_e is better than increasing N. Several commercial low-profile cores are recommended in TABLE III. This paper introduces a new index V_e/A_e to evaluate the performance of the core shapes for the high frequency inductor design. As long as the window area is enough for the windings, smaller V_e/A_e is more efficient than larger V_e/A_e.

TABLE III
RECOMMENDED CORE SHAPES FOR SOFT-SWITCHING TOTEM-POLE PFC

	Core Shape	A_e(mm^2)	V_e(mm^3)	V_e/A_e(mm)
EE	E32/6/20	130	5380	41.4
	E22/6/16	78.3	2550	32.6
	E18/4/10	39.3	960	24.4
ER	ER32/6/25	141	5400	38.3
	ER23/3.6/13	50.2	1340	26.7
EQ	EQ30	108	4970	46.1
	EQ25/LP	89.7	2370	26.4

D. Multi-Phase Interleaving and the Control

For the soft-switching totem-pole PFC, the high current ripple causes challenges for the design of the input filter. Multi-phase interleaving is a possible solution. Fig. 13 shows an example of

the comparison of the current ripple without dual-phase interleaving and the current ripple with dual-phase inter-leaving. The input current ripple is significantly reduced with the interleaving.

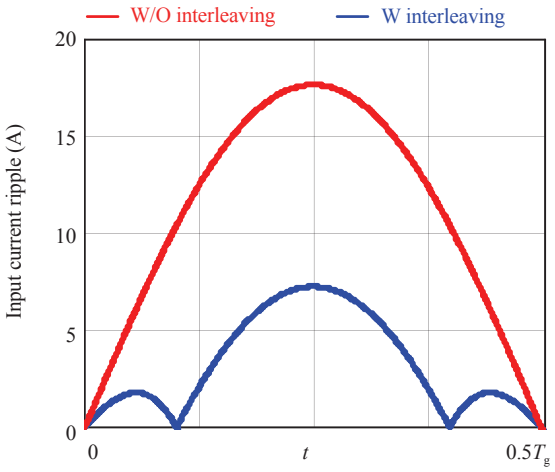


Fig. 13. Comparison of the input current ripples: V_{in}=240 VAC, V_{out}=400 V, P_o=1.6 kW.

However, the multiphase interleaving PFC introduces an additional challenge in control because the control is a variable frequency one. Two kinds of control methods for the multi-phase CRM Boost PFC have been utilized to address this issue.

The first method is the open-loop methods [45], [46]. Using the open loop control methods, there is a master phase, and the other phases are slave phases. The master phase is controlled like a one-phase PFC. The slave phases' turn on or turn off instants are synchronized to the turn on or turn off instant of the master phase with a phase delay. The delay time is generated based on the detection of the master phase's switch-ing frequency. Then, the slave phases turn off or turn on instants are self-controlled like a one-phase PFC. The open loop methods are easy for implementation. However, the slave phases' soft-switching or current control could be lost during the transient.

The other kind of method is the closed-loop method [34], [35], [46], [47]. In the closed-loop method, the multiple phases are controlled with soft-switching. At the same time, an additional feedback control adjusts the interleaved phases between the multiple phases. The closed-loop method requires high speed calculation if the frequency is in the MHz range. Otherwise, the delay of the phase-interleaving feedback contro-ller would cause the oscillations of the currents [46]. On the contrary, the open loop methods do not have this risk even if using lower speed digital processor [46].

In general, for high frequency multiphase GaN totem-pole PFC, the open loop interleaving methods are better than the closed-loop interleaving methods [46].

E. Efficiency and Density

As a proof of concept development, a 3.2 kW GaN dual-phase soft-switching totem-pole PFC is developed and tested. The picture of the prototype is shown in Fig. 14. The size is 7.9x1.8x1.8 inch^3. The power density achieved is 130 W/inch^3. The frequency distribution under full load condition is shown in Fig. 11. The maximum frequency under full load is 900 kHz.

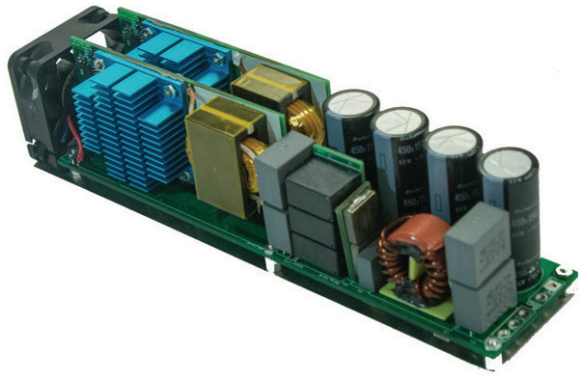
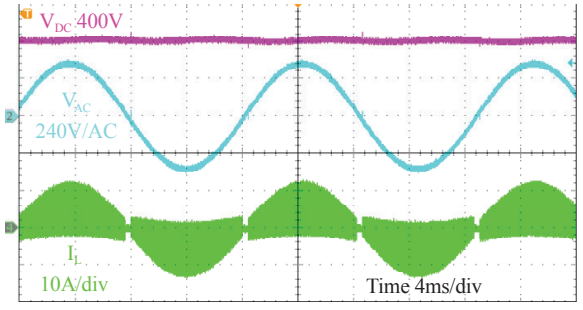
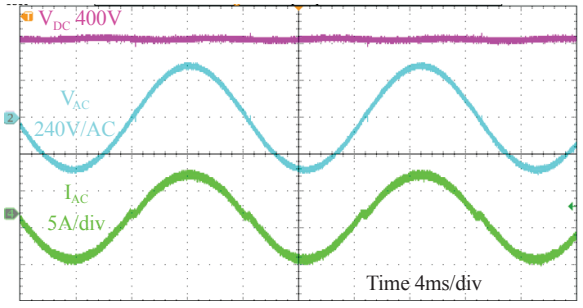


Fig. 14. Protype of a 3.2 kW GaN dual-phase soft-switching totem-pole PFC.

The testing waveforms for one phase are shown in Fig. 15. During the zero-crossing time of the AC voltage, the voltage second of the inductor is almost zero. The inductor current is easily distorted during the zero-crossing time. Since this issue also exists in the conventional Boost PFC, all existing solutions [48]-[51] to this issue for conventional Boost PFC can be used for the totem-pole PFC. All previous methods focus on improving the current dynamic response. Hence more complexities are introduced in the control. Another simple and effective method is to add a 20~40μs blanking time for all gating signals during



(a)



(b)

Fig. 15. Testing waveforms for one phase soft-switching totem-pole PFC under the conditions: v_{in}=240 VAC, V_{out}=400 V, P_o=1.6 kW, L=9.5 μH.

TABLE IV
COMPARISON OF SOFT-SWITCHING PFC

Topology	Company/Institution	Power (kW)	Frequency Range (kHz)	Efficiency of half load (%)	Efficiency of full load (%)	Power Density (W/inch^3)
2 Phase CRM Si-based Boost PFC	Ilmenau University of Technolog [52]	1	50-500	97.5	97.5	<50
2 Phase ZVS GaN Totem-pole PFC	CPES [1]	1.2	1000-2500	99	98.8	700 (without bulky cap, controller, fan)
	Author's group	3.2	250-900	99.05	99	130

the AC voltage zero crossing time. During the blanking time, all the gating signals are zero. This method still introduces some small current distortion, however the THD standards still can be satisfied. As shown in Fig. 15(b), the AC current is clamped to zero during the zero-crossing time using the blanking method.

The efficiency curve for one phase of the prototype is shown in Fig. 16. The efficiency is over 99% from half load to full load. The comparison of the soft-switching PFCs is shown in TABLE IV. The dual-phase interleaving ZVS GaN totem-pole PFCs show superior performance compared with the CRM Boost PFC.

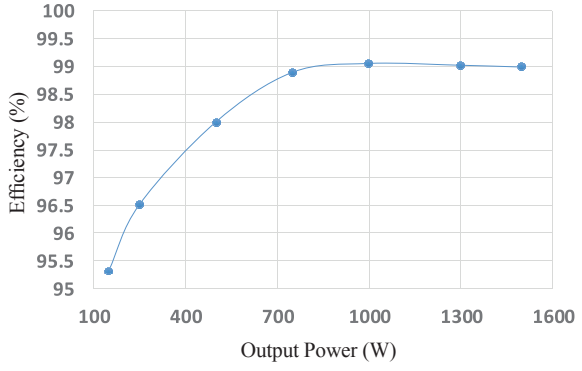


Fig. 16. Efficiency curve of one phase of the prototype under the conditions: v_{in}=240 VAC, V_{out}=400 V, L=9.5 μH.

VI. CONCLUSIONS

In this paper, the technologies, control and performances of the GaN totem-pole PFC are reviewed. Several conclusion remarks can be made. First, the currently available 600 V GaN devices have shown superior perfor-mances compared with the Si SJ MOSFETs, especially the zero reverse-recovery loss in the enhancement-mode GaN FETs. By eliminating the reverse recovery issue, the GaN totem-pole true-bridgeless PFC is poised to be the next generation PFC solution with ultra-high efficiency and high power density. It can work under CCM hard-switching mode with over 99% efficiency. However, the limited switching frequency of hard-switching GaN totem-pole PFC does not improve the power density compared with the CCM Si Boost PFC and clearly shown in Fig. 17. The ZVS GaN totem-pole PFC can push the switching frequency well above MHz level while maintaining 99% efficiency. A 3.2 kW MHz 99% efficient ZVS GaN totem-pole PFC developed by the author's group achieves an amazing 130 W/inch^3 power density, which is more than two times of the power density of the best CCM GaN totem-pole PFC. In addition, this paper also points out that the hardware design and the control of the CCM GaN totem-pole PFC are similar to those of the Boost PFC. The soft-switching totem-pole PFC can achieve full input-and output-voltage range ZVS using the dual-mode ZVS control. The multiphase inter-leaving technique significantly reduces the input current ripple and is well suited for higher power PFCs. The high frequency ferrite materials and core shapes are also reviewed and recommended.

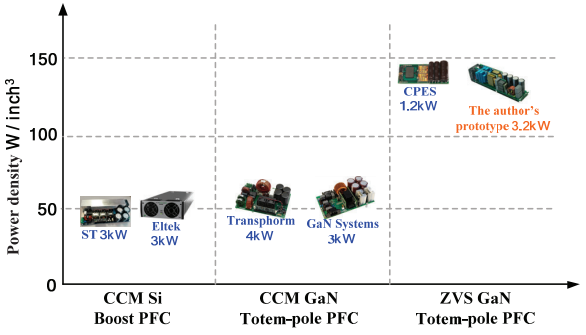


Fig. 17. Comparison of the power density.

ACKNOWLEDGMENT

The author's work was conducted with the use of GaN device samples donated by Navitas.

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The Past, Present, and Future of Power Electronics Integration Technology in Motor Drives

Thomas M. Jahns and Hang Dai

***Abstract*—The physical integration of power electronics and electric machines to form integrated motor drives (IMDs) eliminates the need for special enclosures and connecting cables in order to achieve mass, volume, and cost savings. The objective of this paper is to examine the future of integrated motor drive technology by first reviewing the history of IMD products from the 1960s to today, highlighting both the reasons for their success as well the significant technical obstacles that they had to overcome. Special attention is directed to the application of IMD technology to electric vehicle traction motor drives during the past 15 years. A long-term vision for IMDs is presented that calls for embedding the drive electronics directly inside the machine enclosure. In keeping with this vision, wide-bandgap (WBG) power semiconductor switches (SiC and GaN) offer exciting prospects for shrinking the size of power converters and simplifying their cooling requirements. New concepts for applying this WBG technology to IMDs are introduced, including revived interest in PWM current-source inverters. In the concluding section, a variety of other promising technologies are introduced that will be critical to realizing the full potential of integrated motor drives.**

***Index Terms*—Current source inverters, high-temperature electronics, integrated motor drives, modular motor drives, power electronics integration, wide bandgap power semiconductors.**

I. Introduction

THE concept of combining an electric machine and power electronics into the same physical structure to form an integrated motor drive (IMD) is far from new. In fact, as discussed in this paper, precursors of today's integrated motor drives date back to the earliest days of solid-state power electronics, not long after the earliest generation of germanium and silicon power semiconductors appeared in the marketplace. Despite the significant number of IMDs that have been successfully commercialized since that time, integrated motor drives continue to occupy primarily niche applications that make up a small fraction of all of the applications served by conventional adjustable-speed motor drives.

Fig. 1 highlights some of the physical differences between conventional and integrated motor drives, providing a convenient launch point for discussing the principal motivations

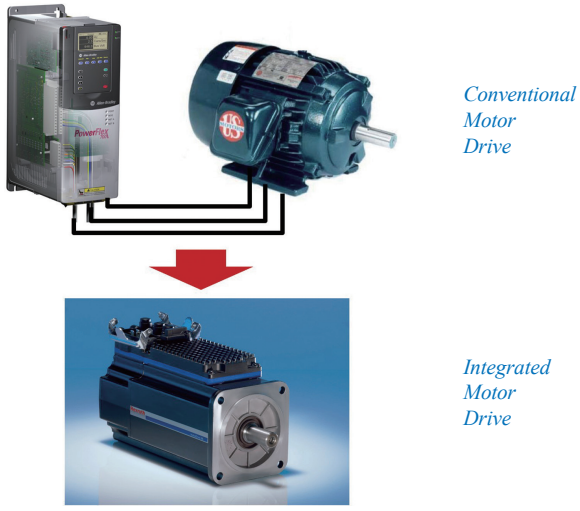

Fig. 1. Integrated motor drive concept contrasted with conventional drive (Image sources: Rockwell Automation, US Motors, Bosch Rexroth).

that continue to inspire broad interest in IMD configurations as candidates for new applications. For conventional motor drives, all of the control and power electronics (referred to henceforth as the drive electronics) is packaged in a separate housing structure that is connected to the machine by electrical cables. This configuration allows the drive electronics to be mounted in a convenient location and environment that may be separated from the machine by distances ranging from <1 meter to much longer distances >1 km. Motivations for adopting the IMD configuration with the machine and drive electronics in the same enclosure include the following factors, not necessarily in prioritized order:

- *Reduced mass:* A number of motor drive applications such as those in aviation (e.g., actuators, pumps, compressors) place a very high premium on mass minimization, so that eliminating the need for a separate drive enclosure and connecting cables is highly desirable.
- *Reduced volume:* Although closely related to the mass reduction objective, some applications such as electric hand tools place a very high priority on minimizing volume, making structural integration increasingly important as the tool power ratings grow.
- *Higher efficiency:* Many existing pump and fan drives continue to use fixed-speed, line-fed induction motors plus various forms of mechanical throttling to provide adjustable fluid and air flow rates. If these machines can be conveniently retrofitted with IMDs that fit into the same space as the machine without a separate drive enclosure,

Manuscript received August 18, 2017. This work was supported by the Wisconsin Electric Machines and Power Electronics Consortium (WEMPEC).

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00019

impressive system energy efficiency improvements that exceed 50% in some cases can be achieved that rapidly pay back the IMD's price premium.

- *Lower cost:* There are multiple potential paths to cost savings opened by IMDs. One of them is directly linked to the major system efficiency improvements described above that will significantly reduce the life cycle energy costs compared to fixed-speed operation, yielding cost savings that exceed the IMD's price premium. A second opportunity anticipates the day when the cost premium of the integrated power electronics needed in IMDs is exceeded by the cost of the eliminated enclosure and interconnecting cables in a conventional motor drive.
- *Improved manufacturability:* The opportunity to supply adjustable-speed motor drives packaged in a single assembly rather than two housings with interconnecting wire harnesses is very appealing to original equipment manufacturers (OEMs) of products such as automobiles and household appliances who are able to simplify their manufacturing process when installing the IMDs.
- *Improved fault tolerance:* As discussed in more detail later in this paper, the integrated motor drive concept lends itself to modular implementations and inverter topologies that hold promise for significantly improving the fault tolerance of the IMDs compared to conventional motor drives, particularly when PM synchronous machines are being used.

Although it is highly unlikely that all of these motivating factors would ever be present for any specific application, subsets of these factors appear sufficiently frequently in real-world motor drive applications that IMD-based solutions have been proposed, implemented, and successfully commercialized in a variety of special applications during the past 50 years. This success is particularly noteworthy since the limitations of power electronics during this period have generally worked to the disadvantage of the IMD implementation. This observation raises hope that advances in power electronics technology that are either now being commercialized or approaching on the horizon (see Section V and VI) will significantly improve the attractiveness of future IMD-based products.

The objective of this paper is to present a vision for the future of integrated power electronics applied to machine drives by reviewing the past, present, and future trends in integrated motor drive technology. Early landmark developments in the history of IMDs are reviewed in Section II, while Section III is devoted to reviewing more recent IMD developments that have appeared in traction drives for hybrid- and battery-electric vehicles during the past fifteen years leading up to the present.

Transitioning from retrospective to prospective, Section IV is devoted to presenting a vision for the future of IMD technology and a discussion of key technical challenges. Technology advances affecting all aspects of the IMD drive electronics are addressed in Section V, including major technology trends that are destined to have an impact on several of these technical challenges. The expected impact of wide bandgap (WBG) power semiconductor technology on future IMDs is singled out for special attention. Progress towards developing the Integrated Modular Motor Drive (IMMD) concept is summarized along with a discussion of the potential benefits of adopting PWM current-source inverter topologies using WBG power switches in future integrated motor drives. Following a condensed review of some important technology developments that affect other components in the drive electronics, the paper concludes in Section VII with some final observations about the future of IMD technology, including the multi-disciplinary skills required of future power electronics and motor drive engineers in order to accelerate this development process.

II. Milestones in IMD Development History

This section is devoted to reviewing some of the milestone developments that have resulted in production IMD equipment during the past 50+ years. A discussion of these noteworthy achievements serves to highlight both the motivations that inspired these integrated motor drives as well as the contemporaneous developments in power electronics technology that made these IMDs possible. These developments are presented in roughly chronological order in order to make it easier to identify the technology progression that made it technically feasible to develop more sophisticated IMDs as the years passed.

A. Automotive Alternators (1960)

The automotive alternator chosen for the first example actually does not qualify as an integrated motor drive, but it is included because it represents a critical precursor of the IMDs that follow in this section. More specifically, the power electronics consists of 6 (or more) diodes in an uncontrolled full-wave bridge configuration without any controlled power switches needed to synthesize variable-frequency ac voltage waveforms. The close linkage between automotive alternators and IMDs lies in the fact that these diode devices are mounted inside the alternator housing in close proximity to the Lundell claw-pole synchronous alternator

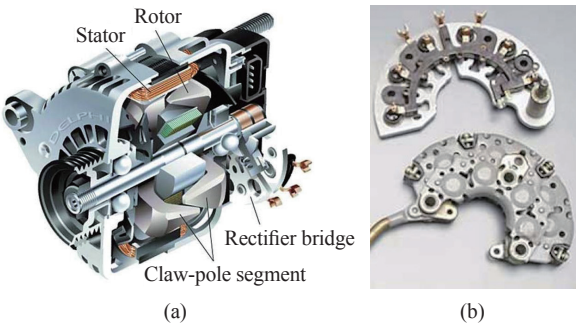


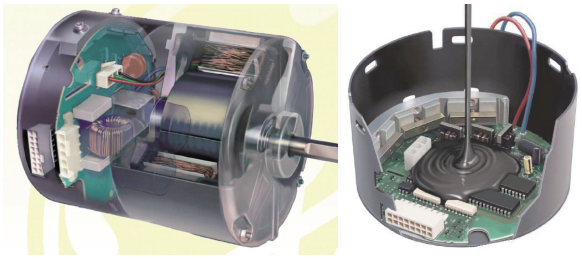
Fig. 2. Modern automotive alternator: (a) cutaway view; (b) 2 production rectifier units [1].

machine, exposing them to the elevated thermal and vibration conditions that accompany this mounting configuration. A cutaway view of a typical modern automotive alternator is provided in Fig. 2(a) and Fig. 2(b) provides a view of two different production versions of the rectifier units [1].

Chrysler installed the first production automotive alternators into their 1960 Valiant model, which occurred only approximately 5 years after silicon power diodes first became commercially available. Despite the early production state of these diode devices, they were packaged in metal cans that allowed them to operate reliably with case temperatures up to 160 °C. Today's silicon diode rectifier installed in automotive alternators have maximum operating case temperatures of 200 °C. The power ratings of these alternators have also increased substantially from less than 500 W in the 1960s to >1.5 kW today. The resulting thermal management challenges are significant, resulting in modern designs using either forced air or liquid cooling. The commercial success of these automotive alternators is truly impressive, with total cumulative production numbers that are conservatively estimated to be in the range of hundreds of millions [2].

B. Electronically-Commutated Motor (ECM) Blower Fan Drive (1987)

One of the first major IMD products developed for residential use in Heating, Ventilating and Air Conditioning (HVAC) applications was the Electronically-Commutated Motor (ECM), first released as a product by GE in 1987 [3]. The ECM was designed for use in residential and light commercial HVAC products such as furnace blowers where they provided a means of improving overall furnace system efficiency and comfort by providing adjustable-speed air flow to the living spaces instead of conventional on-off thermostat-based control with a fixed-speed blower. The basic configuration of the ECM consists of a PM synchronous motor mounted in its own housing with two end bells, attached to a cylindrical shell having the same diameter as the motor housing that contains all of the drive electronics. Fig. 3 provides both a transparent view of the ECM in Fig. 3(a), and a view of the ECM drive electronics in Fig. 3(b) [4]. ECM products were developed with several power ratings that fell in the range between 300 W and 1 kW.



(a) (b)

Fig. 3. Electronically-Commutated Motor (ECM) showing: (a) a transparent view of the ECM; and (b) a view of the ECM drive electronics mounted in a concentric shell housing [4].

As indicated in Fig. 3(a), the ECM uses a surface PM machine with ferrite magnets. The machine stator incorporates concentrated windings that deliver trapezoidal back-emf waveforms so that the motor can be excited as a so-called brushless dc machine with six-step current waveforms. This configuration offers advantages for simplifying the control algorithm and sensor requirements, making it possible to use the zero-crossings of the back-emf voltage waveforms for rotor position sensing.

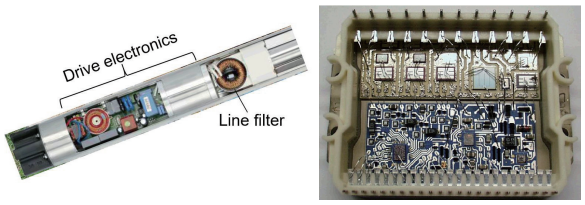
Fig. 3(b) reveals that the ECM was designed to use mostly discrete parts including 6 transistor switches (plus anti-parallel diodes) in individual TO-220 packages that are clamped to the side of the shell housing for air cooling.

Other competitors responded with their own versions of ECM blower drives that, in some cases, used induction machines instead of PM machines. Unfortunately, the ECM products were not immediately embraced by the HVAC industry due to a combination of factors including early reliability problems and an initial lack of receptiveness by HVAC equipment distributors and field repair staff. Eventually these problems were overcome, and ECM-class IMDs are now being widely accepted by the HVAC industry in North America in many of their products including air handlers, furnaces, heat pumps, air conditioners, and refrigeration equipment.

C. Submersible Water Pump (1999)

Grundfos, an international pump manufacturer with headquarters in Denmark, was responsible for another milestone in the history of IMD engineering when they developed and installed an integrated motor drive into one of their submersible water pump products that was introduced into the marketplace in 1999. Adoption of an adjustable-speed motor drive made it possible for Grundfos to deliver constant water pressure to the users in spite of changes in the water flow demand. Mounting the motor and the drive in the submersible pump unit underground made it possible to simplify the power cabling required in the well shaft while using the pumped water as a plentiful and effective coolant for the motor and the drive electronics [5].

Developing the IMD for this application required it to be designed to fit in a cylindrical tube with a diameter of 7.6 cm (Fig. 4). A high-speed surface PM synchronous motor was selected for this special application, and a "wet rotor" design was adopted that required the water to flow through the full length of the machine in the airgap, cooling both the stator and rotor in the process. A compact implementation of the drive electronics was achieved by means of a custom-designed (1 or 2.2 kW) hybrid integrated circuit that incorporated a three-phase inverter, single-phase rectifier, and power factor correction stage. This hybrid circuit module was mounted on an arc-shaped heat sink that adhered to the stainless steel pump casing tube, taking advantage of the cooling capacity of the pumped water that flowed over its surface. Although the IMD unit raised the cost of the unit, the constant-pressure capabilities that it provides have made it a success in the



(a) (b)

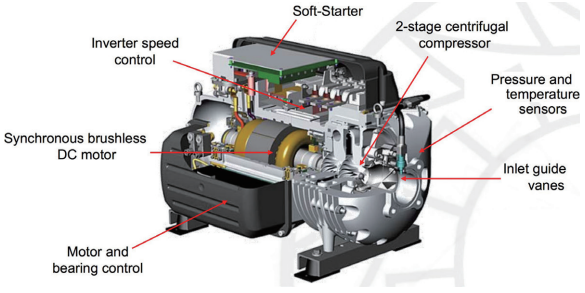
Fig. 4. Grundfos submersible pump: (a) cutaway view of pump unit showing key IMD components ; and (b) Hybrid integrated circuit containing inverter, rectifier, and power factor correction power electronics (*Source: Grundfos*).

marketplace since it was first introduced in 1999.

D. High-Speed Chiller Compressor (2000)

In the early 2000s, a high-speed chiller compressor product was introduced into the HVAC marketplace that incorporated an integrated motor drive as a key component. The chiller unit was manufactured by Turbocor, an Australian company, and developed in partnership with CSIRO (Commonwealth Science and Industrial Research Organization), an agency supported by the Australian federal government. This product represents a significant milestone in the commercial/industrial refrigeration business because it demonstrated the ability to significantly shrink the chiller mass and volume by replacing a lower-speed (<5000 rpm) reciprocating, screw, or scroll compressor with a high-speed centrifugal compressor designed for operation at 48,000 rpm [6].

A high-speed PM synchronous machine is mounted on the same shaft as the compressor (i.e., no gearbox) and the drive electronics is wrapped around the machine to form the IMD as shown in Fig. 5. Air and water are used for cooling in different models of the chiller that are available with ratings up to 700 kW (200 ton cooling) from Danfoss Turbocor. Another innovative feature of this chiller is the use of magnetic bearings for suspension, giving the chiller the special distinction of being oil-free. In addition to the mass/volume reduction, the combination of centrifugal compressor and adjustable-speed capability makes it possible for these chillers to deliver significant improvements in their Coefficient of Performance (COP) values under partial-load conditions compared to conventional chillers using screw compressors.



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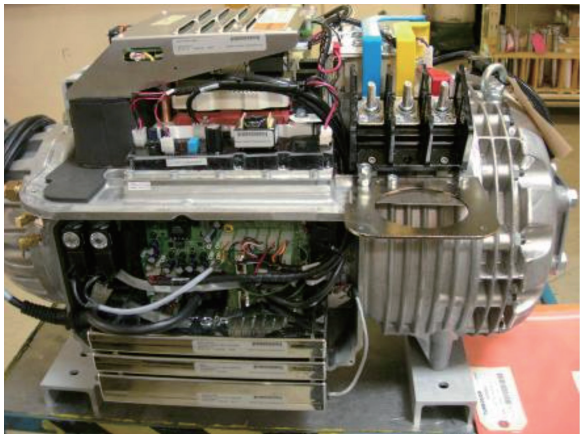
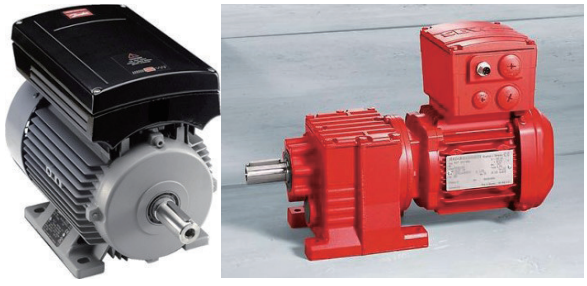


(b)

Fig. 5. Danfoss Turbocor chiller compressor: (a) Cutaway view of compressor unit identifying key components including IMD subassemblies; (b) Partially disassembled compressor exposing drive electronics [6].

E. Industrial-Grade Integrated Motor Drives (1990s to Today)

During the past 25 years, a number of manufacturers of conventional motor drives have developed integrated motor drive product lines intended for general-purpose industrial applications including pumps and fans/blowers that derive performance improvements and energy cost savings benefits from adjustable-speed operation. These units can vary significantly in shape and volume, but nearly all of them adopt a relatively conservative IMD configuration in which the drive electronics is mounted in an enclosure that is physically attached to the machine frame. As a result, the drive is easily visible as an appendage to the machine it is exciting (see Fig. 6). Advantages of this design approach include the fact that the drive electronics is isolated more completely from the thermal and vibrational challenges imposed by the machine compared to IMD designs in which the drive electronics is integrated inside the machine housing.



(a) (b)

Fig. 6. Examples of IMD products for industrial pump/fan/blower applications: (a) Danfoss VLT DriveMotor [7]; (b) SEW Eurodrive MOVIMOT gearmotor product incorporating gearbox together with IMD [8].

Since these IMD units are intended for use with conventional pumps and fans, induction machines are typically adopted for their designs with ratings from 0.5 to 10 kW, although product offerings using PM synchronous machines are also available. Combining the motor and drive into the

same assembly is appealing to industrial customers who would like to retrofit existing fixed-speed pumps and blowers with adjustable-speed capabilities, without having to worry about finding separate wall or floor space for mounting a conventional stand-alone motor drive.

Although these industrial IMD units have been available for many years, their commercial success has been rather limited when considered as a fraction of all industrial motor drives for pump and fan applications sold each year with ratings less than 10 kW. The reasons for their limited marketplace success are varied, but it is generally acknowledged that many potential customers are concerned that the drive electronics will fail long before the machine, making it necessary for customers to pay the higher cost of replacing both the machine and the drive whenever a drive failure occurs. While it can be argued that the justification for this concern is getting weaker each year as drive reliability continues to improve with time, it nevertheless highlights the fact that high temperature and vibration are almost always among the most difficult technical challenges faced by IMD designers. Stated differently, the act of purposely mounting the drive electronics in close physical proximity to the machine significantly aggravates the challenge of designing IMD products that can meet increasing customer expectations for higher reliability in the motor drives that they purchase.

F. Industrial Automation Servo Drives (2006)

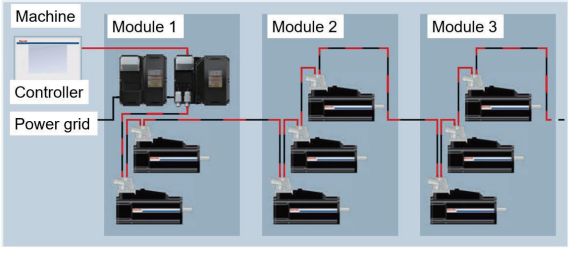
Industrial automation servo drive applications offer an attractive opportunity for IMDs to demonstrate and capitalize on the special advantages that they can offer. Using the conventional approach, an automated manufacturing line with many servos has a separate drive unit for each servomotor, and these drive units are all mounted together in a cabinet, requiring a separate set of multi-phase electrical cables to connect each motor to its dedicated drive. However, if each servomotor is co-packaged with its drive electronics, then only dc power and the servo commands have to be distributed to each of these integrated servomotors. Since large numbers of servomotors can draw their dc power from the same bus in a "daisy-chain" configuration (Fig. 7(a)), the reduction in required cabling between the controller cabinet and all of the servomotors can be significantly reduced, saving cabling cost, mass, and volume, as well as valuable installation time and cost. This opportunity makes the IMD approach particularly attractive and cost-effective for manufacturing automation applications [9].

In 2007, Bosch Rexroth introduced their IndraDrive Mi product line that integrates high-performance PM synchronous servo machines with their drive electronics into compact IMD configurations (Fig. 7(b)). Although the servomotor and the drive electronics are actually separate units, they have been designed for convenient interconnection into a tightly packaged configuration. While the motor itself can be cooled by natural convection, forced air ventilation, or liquid, depending on the model selection, the drive electronics unit is mounted on one of four axial surfaces of the machine frame that serves as the heat sink for dissipating the power converter losses. The IndraDrive power electronics is capable of delivering peak output power values up to approx. 12 kW. The IndraDrive servo product line has been sufficiently successful that it has motivated competing servo manufacturers to develop their own IMD-based servo drives.

G. Hand Dryer Air Blower (2013)

The final IMD-based commercial product highlighted in this section is the Airblade Tap hand dryer developed by Dyson Ltd and first introduced in 2013 (Fig. 8(a)). At the heart of the powerful air blower is a 1.6 kW high-speed surface PM synchronous machine that spins at 100,000 rpm, resulting in a very compact integrated air blower unit including the motor, drive electronics, and blower impeller that fits inside an 85 mm diameter cylindrical shell (Figs. 8b and 8c). The single-phase H-bridge inverter used to excite this machine is built on a printed circuit board mounted immediately below the machine to form an IMD. The blower unit is designed to accelerate the impeller from 0 to 90,000 rpm within 0.7 sec, and deliver an airflow speed of 717 km/h during full-speed operation at 100,000 rpm [10].

While the high speed and resulting high power density of this air blower IMD gives it some unique performance characteristics, several of its basic layout and construction features are similar to those found in other IMDs developed for use in a variety of other residential and commercial applianc-



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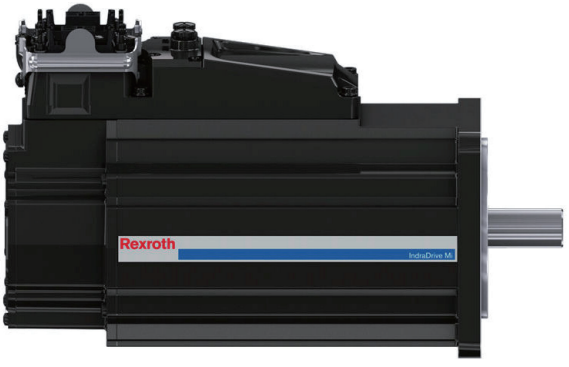


(b)

Fig. 7. IMD used in factory automation servo drives: (a) Servo drive interconnection scheme using only a single cable to distribute both dc power and communications; (b) Bosch Rexroth IndraDrive Mi servo [9].

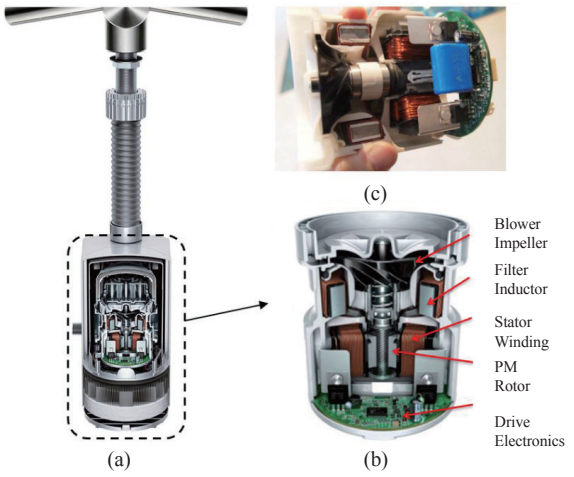


Fig. 8. High-speed hand dryer blower unit: (a) Cutaway drawing of Dyson Airblade Tap hand dryer; (b) Cutaway drawing of 1.6 kW blower IMD unit including impeller; (c) View of cutaway blower hardware [10].

es. For example, many types of refrigeration units require circulating fans with low power ratings < 0.75 kW that are appealing candidates for IMD implementations. Packaging the drive electronics in the same enclosure as the motor and blower enables major suppliers to sell integrated blowers to large appliance original equipment manufacturers (OEMs) that can be easily and quickly installed as single units during the appliance manufacturing process, rather than as separate motor and drive units connected by an electrical cable. This is a trend that is likely to continue growing during coming years in a variety of manufactured goods including hand tools and automotive accessories in addition to appliances.

III. Review of IMD Developments for Automotive Traction Drives

One of the application areas that has actively motivated the development of several new integrated motor drive concepts at high power levels >25 kW during recent years has been traction motor drives used in the powertrains of hybrid- and battery-electric automobiles. This section is devoted to reviewing several of the most noteworthy IMD technology developments for the powertrains of on-road electrified vehicles during the past 15 years that help to highlight both the motivating factors for IMD adoption as well as the likely directions for future IMD technology development.

A. Merging of Powertrain Hardware with Drive Electronics

When it was introduced in the late 1990s, the Toyota Prius adopted a configuration that mounted all of the hybrid powertrain control electronics into a dedicated enclosure that is separated from the engine, two PM machines, and planetary gear assembly that comprise their power-split powertrain architecture, as shown in Fig. 9(a). This required large electrical power cables and heavy-duty connectors to link these two

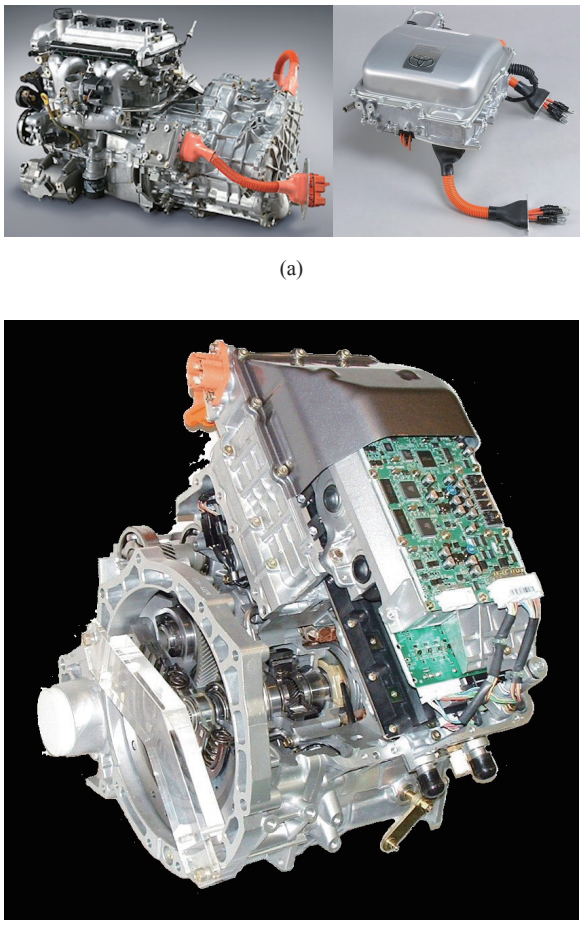


Fig. 9. Hybrid power-split integration evolution: (a) 2000 Toyota Prius configuration with separate powertrain hardware and controller enclosures; (b) 2004 Ford Hybrid Escape with integrated powertrain and drive [11].

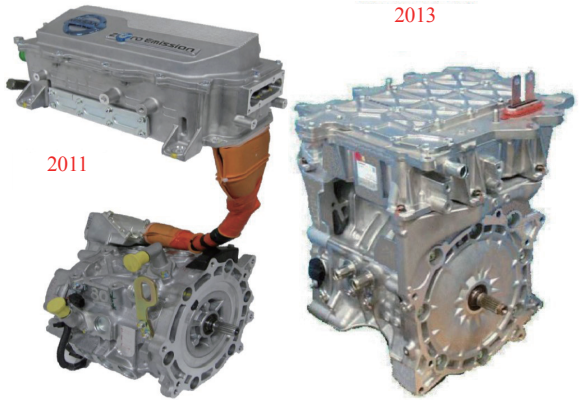
assemblies that are very apparent in Fig. 9(a), resulting in a negative impact on both the powertrain cost and reliability.

Ford Motor Co. worked with Aisin Seiki, a major Japanese automotive supplier partly owned by the Toyota group, to develop the powertrain transaxle for the 2004 Ford Hybrid Escape that used the same basic power-split architecture as the Prius. However, the enclosure for the powertrain control electronics was combined with the housing for the rest of the powertrain hardware to form a single merged transaxle assembly, as shown in Fig. 9(b). The inverters for the two interior PM machines have a combined peak power rating of 115 kW. The power electronics is cooled by water and the two machines are cooled by automatic transmission fluid (ATF), with a heat exchanger between the two coolant fluids integrated into the transaxle assembly. Rubber vibration isolators were used to help protect the powertrain control electronics from excessive engine vibration [12].

Advantages of the merged transaxle design include elimination of the external power cables and connectors that were required in the Prius configuration discussed above. The merged transaxle configuration used in the Ford Hy-

brid Escape was sufficiently successful that the same basic configuration was adopted again in the Ford Hybrid Fusion introduced four years later in 2008.

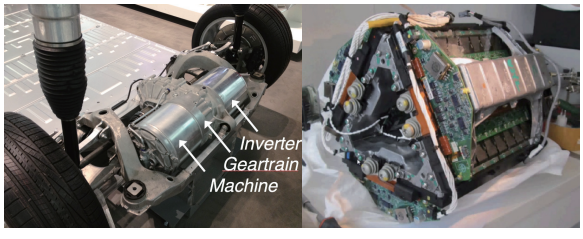
In more recent years, this trend towards merging the powertrain hardware and electronics into the same assembly enclosure has been occurring in other electrified vehicles as well. One documented example of this evolution is the development of the second-generation powertrain for the Nissan Leaf battery-electric vehicle. Like the Toyota Prius, the first-generation Leaf introduced in 2011 used separate enclosures for the powertrain hardware and electronics, connected by an external power cable. The second-generation Leaf powertrain introduced two years later in 2013 merged the two enclosures together to eliminate the external cable, as shown in Fig. 10. Nissan engineers have described that an additional advantage of this re-design was a net reduction in the total electric powertrain mass by >10% [13].



(a) (b)

Fig. 10. Evolution of Nissan Leaf powertrain hardware and control electronics to integrated assembly in 2nd generation (2013) design [13].

Another example of current trends in the evolution of electric powertrain designs towards IMD architectures is the Tesla Model S powertrain that was first introduced in 2012. The powertrain for the Model S battery-electric vehicles (Fig.11(a)) was developed as a rear-wheel-drive transaxle assembly consisting of two cylindrical housings with almost the same diameter and length, one for the induction machine and the other for the inverter, with the geartrain assembly sandwiched between them. The motor and inverter are both rated for 325 kW peak power.



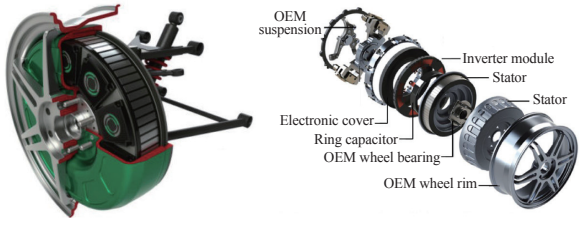
(a) (b)

Fig. 11. Tesla Model S battery-electric vehicle powertrain: (a) Rear axle powertrain transaxle layout [14]; (b) Cylindrical 3-phase 325 kW (peak) inverter without housing [15].

B. In-Wheel Traction Motor Drive (2006)

A more aggressive approach to applying IMD principles has been taken by engineers at Protean Electric in the process of developing an in-wheel motor traction drive. The in-wheel traction architecture differs significantly from that of electric vehicles currently in production because the traction motor is mounted directly inside the wheel hub so that it directly delivers its torque and power to the wheel without needing any transaxle shaft or gearbox. Although the idea of in-wheel traction drives is not new, Protean has been among the most active companies during the past several years developing engineered prototype traction drives that it has used to attract partners/customers for vehicle production opportunities.

Fig. 12 provides rendered drawings of the Protean in-wheel traction drive, including both a cutaway view and an exploded view of their in-wheel drive unit. The unit uses an inside-out surface PM machine with the rotor magnets mounted along the inner circumference of the hub on which the vehicle's wheel is mounted. The Protean in-wheel motor is capable of delivering 1000 Nm of torque and 75 kW of power to the wheel. The stator that excites the spinning rotor hub assembly takes the form of an annular laminated steel core mounted inside the hub. Stator windings are mounted in stator core slots and these windings are excited by an inverter in the early prototype units that is designed to fit inside and adjacent to the annular stator core. In this configuration, the drive electronics has to be sufficiently rugged to survive the hostile environment inside the wheel hub, including very high g-forces, both high and low temperature extremes, as well as exposure to the high levels of dirt, water, and vibration that define typical road conditions [18].



(a) (b)

Fig. 12. Protean Electric in-wheel traction drive: (a) Rendered cutaway drawing of assembled 75 kW unit [16]; (b) Rendered exploded view of key components that comprise the in-wheel traction drive [17].

The in-wheel traction drive architecture offers vehicle designers a combination of both intriguing performance opportunities and challenges that continue to draw attention and debate in the automotive engineering community, but no consensus. While it is uncertain whether the Protean in-wheel traction drives will achieve commercial success, the ambitious nature of their IMD-based design helps to inspire

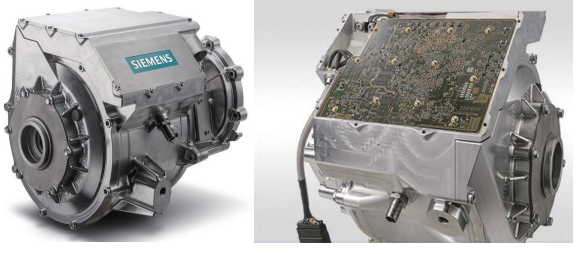
and challenge traction drive designers about the technical feasibility of this approach and the problems that remain to be fully addressed.

C. Integrated Traction Motor Drives

There is growing evidence that automotive traction drive suppliers are taking the integrated motor drive more seriously in their future product plans. An example is the SIVETEC line of traction drive products developed by Siemens. In 2014 the SIVETEC MSA 3300 integrated motor drive was announced with a power rating of 60 kW. Two views of this IMD are provided in Fig. 13, showing the unit both with and without a metal cover over the drive electronics. Comparing this IMD with the earlier examples of merged powertrain hardware and controller units already in production (Figs. 9(b) and 10), some differences are apparent in their appearances: 1) the size of the drive electronics compared to the machine it excites has been reduced noticeably in the newer MSA 3300 unit compared to the Ford and Nissan units; and 2) the extent of the physical integration of the power electronics with the machine is tighter in the MSA 3300 unit.

In addition to these differences that are externally visible, the power electronics in the MSA 3300 is built using power modules in which the power semiconductors are sintered rather than soldered, and wire bonds are replaced with planar interconnect technology [20]. Both of these changes are important steps in the direction of further ruggedizing the power electronics to improve its reliability in more demanding thermal and vibration environments that are typical of IMDs.

Available information from Siemens indicates that their SIVETEC integrated motor drive technology is available using either PM synchronous or induction machines with drive ratings up to 200 kW. This IMD technology has been adopted for use in two of Volvo's vehicles: the XC90 T8 plug-in hybrid sport-utility vehicle, and the C30 battery-electric hatchback vehicle. Neither of these vehicles are in large-scale production as of this writing. Despite the uncertainty about the future production plans for these motor drives, the SIVETEC MSA 3300 represents a significant milestone in the development of integrated motor drive technology for electrified vehicle powertrain applications.



(a) (b)

Fig. 13. Siemens IMD technology for EV traction drives: (a) View of 60 kW SIVETEC MSA 3300 drive unit; and (b) MSA 3300 drive unit with cover removed to expose drive electronics [19].

IV. Future Vision and Technical Challenges

A. Long-Term Vision for Integrated Motor Drives

The review of key milestones in the development of integrated motor drives presented in the preceding two sections has highlighted the impressive progress that has been made during the past 60 years toward increasing the degree of physical integration of electric machines and their drive electronics. The IMD examples that have been highlighted also demonstrate the major positive impact that this technology is already having on a wide variety of applications that range from hand dryers to electric vehicles. For engineers and technologists working in this field, this look backwards in time serves as inspiration for looking forward and asking where IMD technology and commercial development are going next, what future IMDs will look like, and what performance they will be capable of delivering compared to today's IMDs. In other words, is it possible to define a coherent future vision for integrated motor drives that can be used to guide future research and development efforts in this field?

Having viewed the landscape of progress achieved during past generations of IMDs leading up to the present, the highest level of long-term vision defining the expected external appearance and functionality of future integrated motor drives becomes rather apparent. In some sense, this vision is anti-climactic since it predicts that future IMDs will look like the motors of today; without any visible motor drive because it has been absorbed into the motor enclosure (Fig. 14). That is, the vision depends critically on the expected continuation of existing trends towards shrinkage of the volume and mass of the drive electronics. Taken to its conclusion, this trend leads to the complete embedding of the drive electronics inside the machine's enclosure without the need for any increases in the key dimensions of the enclosure. As a result, future IMDs will look like today's motors, with the drive electronics hidden from view somewhere inside the motor enclosure. The exact location of the integrated drive electronics is yet to be determined; it could be in the space currently occupied by the conventional machine's terminal box as suggested in Fig. 14, but it could be in other parts of the machine such as the end bells or stator frame.

The appeal of this future IMD vision is that the key external dimensions, mass, and volume of the motor will change very little from today's motors, but the performance and functionality of the motor will be critically transformed with speed, torque, and/or rotor position control conveniently available at the fingertips (literally) of the users. As indicated in Fig. 14, all of the communications between the user and IMD controls will be accomplished either wirelessly or via the power lines in order to avoid the need for any new signal-level control wiring between the user and the IMD. The user will be able to issue commands and monitor perfor-

Fig. 14. Future vision of integrated motor drives with embedded power electronics.

mance (including diagnostics) using either a control console, a desktop computer, or a smart phone to provide maximum flexibility.

As the drive electronics progressively "disappears" inside the motor enclosure over time and these IMDs become more widely adopted as the baseline norm in many applications, casual users of these "smart" motors will become increasingly unaware of even the existence of the drive electronics. This is the typical and expected fate of any truly embedded technology that becomes so widely adopted yet invisible that, ironically, it becomes increasingly taken for granted by IMD purchasers and users. It will mark one of the ultimate successes of IMD technology when that happens.

B. Key Technical Challenges

Having defined the ambitious long-term vision for integrated motor drives in the preceding section, the next logical step for IMD developers and technologists is to identify the key technical challenges that must be overcome in order to achieve this vision. Here again, consideration of the past history of IMD development milestones presented in Section II and III is instructive for sharpening the focus on the most significant technology barriers that are obstructing future progress. The key technical challenges that emerge from this review, not necessarily in prioritized order which is heavily influenced by application details, are:

- *Reductions in power electronics cost:* Broad adoption of IMD technology in commercial, industrial, residential, and transportation applications depends on advances in power electronics technology that will lead to major cost reductions for integrated power electronics. Materials, manufacturing processes, standardization, and modularization are all expected to be major factors in accomplishing these cost reductions.
- *Overcoming maximum temperature limitations of power electronics:* Technology must emerge that will make it possible for power electronics to withstand the dual thermal threats imposed by placing the power electronics in close proximity to electric machines that can typically operate with hot spot temperatures of 180 °C or higher, while simultaneously packaging the power electronics within progressively smaller volumes that aggravate the heat extraction challenges. This challenge can be dissected into three sub-challenges, as follows:
  - o *Development of higher efficiency power electronics:* Reducing the losses generated by the power electronics represents a highly desirable objective for reducing both the peak temperatures and the IMD energy usage.
  - o *Development of improved thermal management techniques:* More effective heat transfer techniques for conducting the heat losses away from the IMD drive electronics and the machine can play a major role in reducing the peak temperatures in the power electronics.
  - o *Development of higher-temperature power electronics:* Development of power electronics that can reliably tolerate extended operation with junction temperatures of 200 °C or higher would represent a powerful asset for overcoming the high-temperature limitations imposed by today's silicon power devices and associated packaging.
- *Major improvements in power electronics reliability:* For IMDs to achieve their full potential, the integrated power electronics must be able to achieve reliability levels that match or exceed that of the electric machine in which it is embedded, despite the hostile environment it experiences. Two of the most demanding aspects of this environment are highlighted here:
  - o *Large repeated temperature excursions:* The power electronics must be able to withstand very high numbers of large temperature excursions that create tremendous stresses at the interfaces between materials with different thermal expansion coefficients in the power semiconductor modules and other critical electrical connection nodes in the power electronics.
  - o *High vibration:* In addition, the power electronics must be able to tolerate long periods of exposure to mechanical vibration caused by the motor and its connected load. Here again, the risks of vibration exposure and damage will tend to be aggravated by embedding the power electronics inside the machine enclosure unless aggressive steps are taken to ruggedize the power electronics as well as to develop vibration absorbers that significantly attenuate the vibration it experiences.

The following section of this paper highlights promising technology developments in different components and subassemblies of the IMD and its drive electronics that raise hope for successfully addressing these technical challenges.

V. IMD Technology Developments

A. Wide-Bandgap Power Semiconductors

One of the most far-reaching and promising technologies now under development in the field of power electronics is

wide bandgap power semiconductors using either silicon carbide (SiC) or gallium nitride (GaN) in place of silicon. Although the impact of WBG power semiconductor technology will not be equally significant in all application areas, it holds potential to be a game-changer that will heavily influence the future of integrated motor drives for reasons discussed below.

1) SiC and GaN vs. Silicon Characteristics

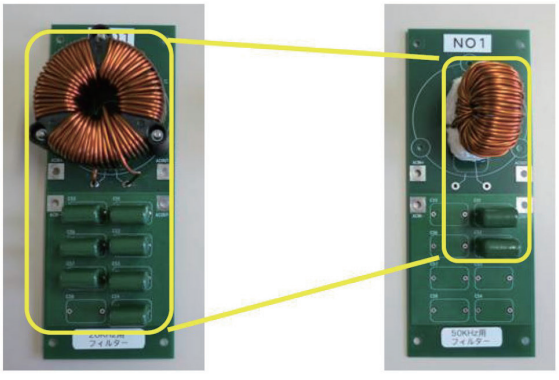
While the idea of replacing silicon with silicon carbide in power electronics dates back to the 1950s, commercial development of WBG power semiconductors did not gain significant momentum until the 1990s [21]. Key motivations for using WBG materials instead of conventional silicon in power semiconductors are opportunities for significant advantages in the areas of operating temperature, efficiency, and switching frequencies. There are a number of review papers available comparing the device-level [21][22], circuit-level [23][24] and system-level [25][26] performance capabilities of WBG and Si devices. The important material characteristics influencing IMD performance are summarized in TABLE I.

As a result of their higher energy bandgap, the WBG devices can have lower leakage current at elevated temperatures, helping to raise the temperature limit of devices made with these materials. The higher breakdown electric field means that WBG devices can be designed to have much thinner drift layers and/or higher doping concentration than silicon devices. Consequently, WBG devices can have much lower on-state resistance than silicon devices with the same voltage ratings. Theoretically, the on-resistance of SiC devices can be 300x less than Si devices with the same voltage rating [27]. TABLE I also shows that 4H-SiC has almost 3 times higher thermal conductivity than Si, which is very beneficial for dissipating heat, making it possible to simplify the thermal management requirements.

Entries in TABLE I also show that the thermal conductivity of GaN on Si substrate is more than 3x lower than that of 4H-SiC. This ratio is so high because it is currently difficult to form high-quality defect-free GaN layers, and these defects result in the reduction of thermal conductivity [28]. Several combined factors enable faster switching of WBG devices including higher saturated electron drift velocity and smaller drift distance for the same blocking voltages. Due to the faster rise and fall times, the switching loss of WBG devices is lower than that of Si power switches, making much higher switching frequencies possible in most cases. Moreover, due to smaller chip dimensions of WBG devices, the gate-to-source capacitance is much smaller than for Si devices, enabling further improvements in the switching frequency [29][30]. The implications of this higher switching frequency on power converter performance are discussed in the next sub-section.

2) Impact of Higher Switching Frequency on Power Converter Mass and Volume

In addition to the size reduction of the WBG devices themselves, implementation of these switches in power converters that can operate at much faster switching frequencies opens opportunities for significant size and mass reduction of the resulting power converters, one of the major objectives for future IMD technology. Illustrating this principle, Fig. 15 shows that the volume of an inverter output *LC* filter can be reduced by more than 2:1 when SiC power switches are used to increase the switching frequency from 20 to 50 kHz [24]. A project supported by the US Department of Energy demonstrated the potential for achieving high power density and efficiency metrics using SiC and GaN power semiconductors, although the focus of that particular project was not on high PWM switching frequencies [31][32]. Mitsubishi Electric has announced development of a SiC-based prototype EV traction drive that achieves a power density of 86 kVA/L for a two-motor hybrid EV, more than 5 times the power density for comparable Si-based power converters now in production [33]. Although promising, few technical details are available at this time that explain how this was achieved.



LC filter for 20 kHz LC filter for 50 kHz

Fig. 15. Comparison illustrating reduction of LC filter footprint made possible by raising the PWM switching frequency from 20 to 50 kHz [24].

Achieving such dramatic size reductions via switching

TABLE I
KEY MATERIAL PROPERTIES OF SI, 4H-SIC AND GAN ON SI SUBSTRATE

Parameter	Bandgap(eV)	Break down elect field. (MV/cm)	Thermal cond. (W/mk)	Sat. electron velocity (10^6cm/s)
Si	1.1	0.25	150	10
4H-SiC	3.2	2.2	490	20
GaN on Si Substratc	3.4	2.0	130	22

frequency increases with a complete power converter is not a simple task. More specifically, the mass/volume reduction of passive components is not a simple inverse-linear relationship with switching frequency when all factors are considered. The dc-link capacitor in a voltage-source inverter (VSI) is a good example. Based only on a capacitance calculation, the required capacitance mass and volume decreases inversely with the frequency (i.e., 1/f). However, in practice, the capacitor's rms current requirements eventually dominate the sizing of these capacitors, changing the results significantly.

As shown in Fig. 16 [28], when the switching frequency is raised higher than a threshold frequency value, the capacitor volume no longer reduces because meeting the rms current requirement prevents it. The curves for three types of capacitors shown in Fig. 16 reveal that this threshold frequency value is lowest for electrolytic capacitors, and significantly higher for both film and ceramic capacitors, reflecting differences in their current-handling capabilities. As discussed later in Section V.C, efforts to achieve major size and volume reductions using WBG switches can benefit significantly from consideration of alternative power converter topologies.

3) Impact of Higher Junction Temperatures on Power Converter Mass and Volume

As noted earlier in this section, WBG devices can operate at much higher junction temperatures than silicon devices. Complementing this feature is the fact that WBG power switches (particularly SiC at the time) exhibit only modest increases in on-state resistance and switching losses as the temperature rises. As a result, the total losses of SiC devices devices are relatively insensitive to temperature increases. These appealing features open opportunities to reduce the thermal management requirements for the power converter if all of the other converter components can be designed to tolerate higher temperatures.

Past studies including both simulation and experiment have demonstrated that SiC power switches make it possible to reduce the mass of cooling systems for an EV drivetrain [34]. The thermal management systems in production hybrid EVs using conventional silicon-based power converter now often employ two cooling loops, one for the internal combustion engine with 105 °C coolant, and a second loop with a lower temperature coolant at 80 °C. Due to the high temperature capability of SiC, it becomes technically feasible to eliminate this lower temperature cooling loop, resulting in a significant volume reduction for the inverter combined with its thermal management system [35]. A separate study for the powertrain of a battery EV using SiC indicates that, with the same thermal management conditions, SiC power modules can achieve current densities that are 2.5x higher than for Si-based power modules [36]. Another study also predicts that a dc/dc power converter (3 to 10 kW) in an EV powertrain can achieve 25% reductions in both volume and mass and eliminate the need for fan cooling by using SiC power devices instead of conventional silicon semiconductors [37].

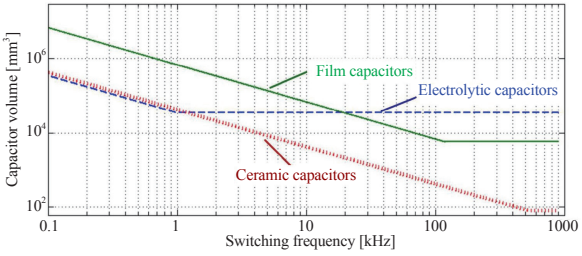


Fig. 16. Calculated plots of VSI dc-link capacitor volume vs. switching frequency for three types of capacitors [28].

Other studies have focused more directly on the opportunities provided by WBG power devices to reduce the mass and volume of the heatsinks by using WBG devices. For example, researchers calculated that the required heat sink for a SiC-based power converter only requires a thermal resistance value of 0.11 K/W, making it possible to use either natural or forced-air convection [38]. In comparison, the heatsink for a Si-based converter with the same power rating requires a much lower thermal impedance of 0.0035 K/W, a value > 30x lower than for the SiC power converter that demands a liquid-cooled heat sink.

As noted earlier in this discussion, the full value of operation with higher junction temperatures offered by WBG power devices cannot be realized unless all of the other electronics, including the device package in which the WBG die is mounted, is designed to operate reliably in higher-temperature environments than they can today. There is a community of researchers in industry and academia who have demonstrated that it is possible to build motor drive inverters using SiC power switches that can operate for extended times with junction temperatures that approach or exceed 200 °C [39]. However, the commercial availability of the necessary components to manufacture high-temperature power converters at sufficiently low cost for high-volume consumer applications is highly limited. This topic will receive more attention later in this paper.

B. Integrated Modular Motor Drive (IMMD)

The heart of the future IMD vision presented in Section IV.A lies with the integration of the drive electronics inside the motor enclosure, referred to in this section as an embedded IMD. Although there are very few commercial IMDs that have adopted such an ambitious approach, there are some researchers who have explored this IMD architecture. For example, a prototype version of an induction motor drive with a matrix converter built into the machine's end bell has been reported [40]. Nevertheless, the literature associated with this aggressive class of embedded IMDs is quite limited. This section presents a summarized discussion of a particular embedded IMD concept known as the Integrated Modular Motor Drive (IMMD) [41] that illustrates some of the specific technical challenges as well as progress that has been made during recent years towards realization of key

aspects of the embedded drive electronics architecture envisioned for future IMDs.

1) Basic IMMD Concept

The Integrated Modular Motor Drive is a concept that was first conceived in 2004 to simultaneously address technical issues associated with the embedded IMD architecture as well as modularization of the machine's stator and inverter. As illustrated in Fig. 17, the IMMD divides both the power converter and the machine stator into individual phase segments. An individual stator core arc segment with its concentrated winding is physically integrated with a single-phase inverter module and its own dedicated controller to form an integrated pole-drive unit. A number of these identical pole-drive units (equal to the number of concentrated stator windings in the machine) are then interlocked and interconnected to form an annular stator assembly that comprises both the IMD's machine stator assembly and the motor drive inverter.

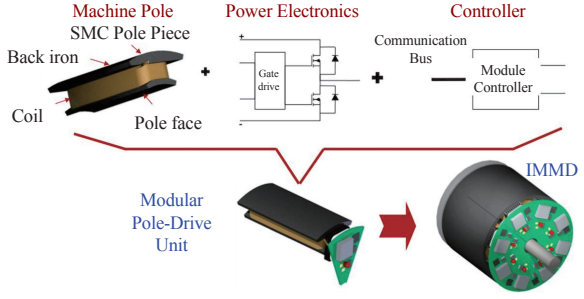
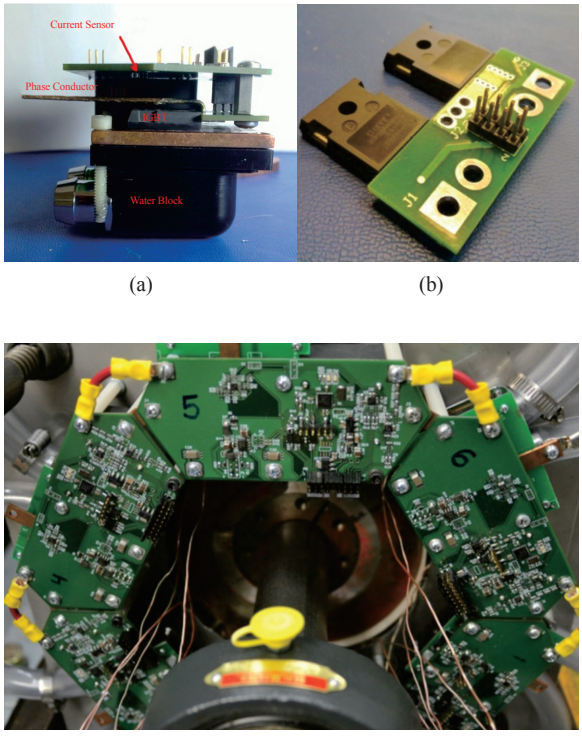


Fig. 17. Basic concept of Integrated Modular Motor Drive (IMMD) [46].

The modularity of this IMMD architecture was introduced with the dual objectives of improving its manufacturability as well as its potential for achieving high fault tolerance [41]. Although these features raise their own set of challenging technical issues, they are not the focus of this discussion. Instead, attention is focused on progress made towards miniaturizing the size of the power converter in order to make it compatible with being embedded inside the machine enclosure. This is accomplished by highlighting the progress that has been made in this direction during two successive generations of prototype IMMD units. More information about preceding technical work on the IMMD concept that set the stage for the two prototype units highlighted in this paper is available in the literature [42]-[45].

2) Second Generation IMMD with Silicon-Based Power Electronics (2014)

Work on developing this prototype IMMD began with a systematic evaluation of machine topologies suitable for a compact IMMD with high power density and efficiency [44]. This investigation determined that a 6-phase, 10-pole PM machine topology was the best candidate for this project. A complete IMMD demonstrator unit shown in Fig. 18(c) consisting of a modular 6-phase, 10-pole, 10 kW(continuous)



(a) (b)

(c)

Fig. 18. 2nd generation Si-based IMMD demonstrator unit: (a) Pole-drive unit side view [46]; (b) Module Si IGBT power stage in phase-leg topology; (c) 6 pole-drive electronic modules mounted in IMMD configuration adjacent to a 6-phase modular PM machine .

surface PM machine with six modular pole-drive electronics modules was designed, constructed, and tested, as shown in Fig. 18(a) [46][47]. This was the first IMMD prototype unit that included a dedicated controller in each module.

The IMMD was designed to deliver a maximum peak power of 18 kW. Each pole-drive unit incorporates a half-bridge inverter phase-leg operating from a nominal 325 Vdc bus using two discrete 600 V IGBTs in TO-247 packages as shown in Fig. 18(b). In addition to the two IGBTs, the power stage includes an RTC temperature sensor, gate connections, and a mounting terminal for the machine phase busbar. Cooling for each phase-leg module is accomplished using an off-the-shelf copper pin-fin waterblock designed for graphics card cooling. As shown in Fig 18(c), the power module is mounted in direct contact with the waterblock to minimize the thermal resistance. High-bandwidth (~10 kHz) current sensing is provided by a linear Hall effect sensor mounted to the bottom of the control board as indicated in this same side-view image.

3) Third Generation IMMD with GaN-Based Power Electronics (2016)

The third-generation IMMD prototype units takes advantage of the benefits that GaN power devices provide for reducing the inverter mass and volume including higher switching frequency and lower conduction losses [28][48]. Like the 2nd generation IMMD discussed above, this proto-

type IMMD unit also uses a 6-phase ac machine, although in this case it is an induction machine. Another difference between the two generations is that the 3rd generation configures the 6 pole-drive units into two 3-phase full-bridge inverters that are in series, rather than in parallel (Fig. 19(a)). This makes it possible to use GaN devices with lower voltage ratings, which reduces the device's on-state resistance and conduction losses. This lower bus voltage for each 3-phase inverter also makes it easier to use small film or ceramic capacitors instead of electrolytic units. This is important since the commonly-used electrolytic capacitors often take up more than 30% of the conventional inverter's total volume, making it a limiting factor for increasing the IMMD's power density. Increasing the PWM switching frequency from 20 kHz in the 2nd generation IMMD to 100 kHz in the 3rd generation unit also plays a valuable role in shrinking the size of the power electronics.

Since the power rating of the induction machine for the 3rd generation IMMD prototype unit is only 1.2 kW, much lower than the 10 kW rating of the 2nd generation PM machine, it is difficult to make direct quantitative comparisons between the two units. However, Fig. 19(b) provide some helpful insight into the size reduction benefits provided by the change from silicon to GaN power switches. This figure compare the size of a preliminary version of the inverter using Si MOSFETs in a 3-phase inverter module switching at 10 kHz to the final version of the 3-phase inverter consisting of 3 single-phase modules using GaN devices switching at 100 kHz (Fig. 19(b)). The significant reduction in the inverter area is very apparent.

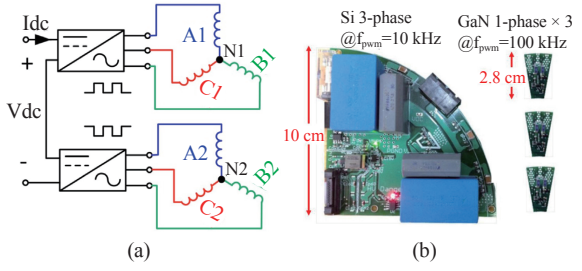


Fig. 19. 3rd generation IMMD: (a) Electrical configuration of 1.2 kW drive using two 3-phase full-bridge inverters in series; (b) Comparison of Si vs. GaN implementations of 0.6 kW 3-phase inverter [28].

Two views of the assembled 3rd generation IMMD prototype unit are provided in Fig. 20. The front view in Fig. 20(a) shows the two 3-phase inverters on the left- and right-sides of the endplate, and the drive controller is mounted in the top quadrant. The 12 GaN switches are mounted in thermal contact with the outer surface of the aluminum endbell which is sufficient to serve as the inverter's heatsink without forced-air cooling. The side view of the IMMD unit provided in Fig. 20(b) shows that the thickness of the IMMD drive electronics is only 1.3 cm. Although this drive electronics unit is mounted on the external surface of the motor's end bell for convenient viewing without disassembly, the drive electronics has been sufficiently miniaturized to be compatible with embedding inside the motor end bell cavity without requiring any changes in the housing dimensions. As a result, comparison of the 2nd and 3rd generation IMMD prototype units provides convincing evidence of the positive impact of well-designed WBG-based drive electronics on the prospects for achieving embedded drive electronics in future IMDs.

C. WBG-Enabled Current-Source Inverters

As discussed in Section V.A, new WBG power semiconductors fabricated using both silicon carbide (SiC) and gallium nitride (GaN) are becoming available that can switch more than 10 times faster than their silicon-based counterparts. There are high hopes in the research community that these new WBG power switches will ultimately deliver major benefits to applications such as IMDs that desperately need breakthroughs that will lead to smaller, lighter, and more efficient power electronics.

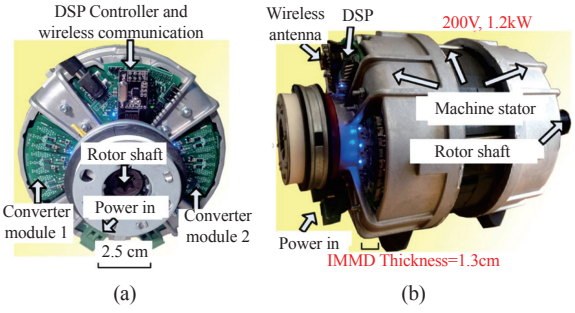


Fig. 20. 3rd generation GaN-based 6-phase IMMD unit rated at 1.6 kW; (a) Front view of IMMD drive electronics; (b) Side view [28].

However, when attempts are made to use these WBG devices as drop-in replacements for silicon-IGBTs in conventional voltage-source inverter (VSI) machine drive inverters with PWM switching frequencies of 100 kHz or higher, vexing problems caused by their much higher *dv/dt* values have emerged, including machine terminal over-voltages and significantly elevated EMI levels [49]-[51]. There are also growing indications that such fast *dv/dt* values can lead to dynamic interations between the drive, connecting cables and the motor load that results in noticeable reduction in efficiency [52]. These problems are sufficiently difficult to solve that they have triggered interest in exploring whether other inverter topologies might offer natural advantages over VSIs when WBG power switches are introduced.

One class of inverter topologies that deserves special attention as a WBG-friendly alternative to the familiar VSI inverter is the PWM current-source inverter (CSI). The PWM-CSI topology has received some past attention from researchers [53], but the topology has been largely ignored by industry because it is not easily compatible with silicon-based power switches. The basic power circuits of both VSI and CSI topologies are provided in Fig. 21 for easy comparison. The replacement of the dc-link capacitor in the VSI with a dc link inductor is one of the three biggest differences. Secondly, the CSI needs filter capacitors at the invert-

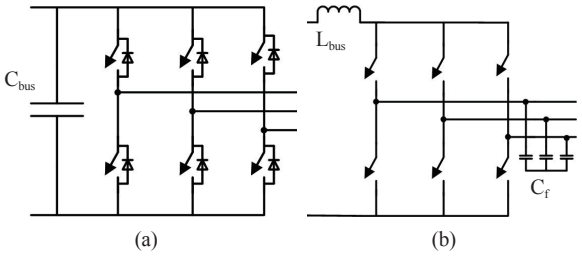


Fig. 21. Basic inverter topologies of 3-phase inverters; (a) VSI; (b) CSI.

er output terminals to make the basic CSI compatible with inductive loads, a feature of most motors. Finally, the presence of the anti-parallel diodes in the VSI and their absence in the CSI reflects the fact that the CSI needs power switches that can block reverse voltages, unlike the VSI. Fortunately, WBG power switches offer some interesting possibilities for realizing reverse-blocking switches that are not easily achieved with silicon-based IGBTs or MOSFETs [54]-[56].

Unfortunately, space in this paper does not permit a full discussion of the potential advantages offered by the CSI inverter topology over the VSI when WBG power switches are introduced. However, some valuable insights into the nature of these advantages can be gained by comparing the terminal voltage waveforms delivered at the output terminals of the two types of inverters. Fig. 22 shows simulated terminal voltage waveforms for a VSI and CSI when the WBG power devices are switching at 200 kHz, more than 10 times the typical PWM switching frequency for silicon power switches. The VSI output voltage waveforms swings between the positive and negative bus voltages at the PWM switching frequency, while the corresponding output waveforms for the CSI are much smoother because of the presence of the output filter capacitors acting together with the dc link bus inductor to filter out much of the harmonic content. Adopting a high PWM switching frequency of 100 kHz or higher plays a key role in reducing the mass and volume of the dc link inductor and the output filter capacitors which are in value ranges that make ceramic capacitor excellent choices.

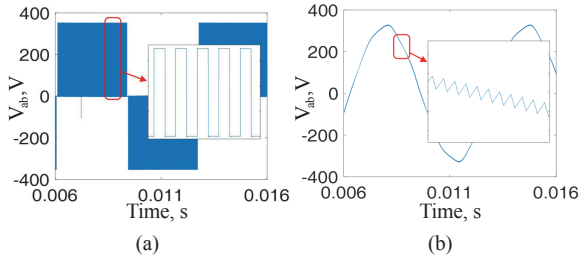


Fig. 22. Simulated output voltage waveforms for two inverters using WBG switches at f_{pwm} = 200 kHz: (a) VSI (without output filter); and (b) CSI.

The sinusoidal output voltage waveforms delivered by the CSI pose much less risk of generating dangerous over-voltages at the motor terminals or unacceptable common-mode EMI levels compared to the harmonic-rich VSI output voltage waveforms. While it is true that the VSI voltage waveforms with their incredibly fast voltage transition would be far less problematic if a 3-phase *LC* filter is added to the inverters output terminals [49][57], the need to add a filter inductor in each phase in addition to the filter capacitances puts the VSI at a mass and volume disadvantage compared to the CSI when the filters are added to the VSI.

In addition to the attractive features noted above in the areas of mass, volume, EMI, resonant over-voltages, and efficiency, there are two more potential advantages for future IMD designs that are worth noting. First, the CSI is an excellent candidate for high-temperature operation compared a VSI. More specifically, the major passive components in the CSI are the dc link inductor and the ceramic capacitors used for the output filter capacitors, both of which are compatible with operation at temperatures >200 °C. In contrast, the dc link capacitor in the VSI is typically implemented using either electrolytic or film capacitors which are limited to maximum temperatures of 125 °C and 170 °C, respectively. The second notable advantage of the CSI when used with a PM synchronous machine is that the absence of anti-parallel diodes across the inverter switches makes the CSI motor drive less vulnerable to highly dangerous short-circuit faults in one of the inverter switches, increasing its fault tolerance [58].

It is acknowledged that preceding discussion in this section has relied on brief qualitative arguments without quantitative evidence that is being provided in other technical papers, some of which are already published [59] and others that are in preparation. However, the key larger point being made is that treating WBG switches as drop-in replacements for silicon IGBTs or MOSFETs may not yield the best solution when there are good reasons to significantly raise the switching frequency or operating temperature. Applying these radically new WBG switches with terminal characteristics that are significantly different from those of the current generation of silicon switches calls for a serious re-evaluation of the most compatible power converter topologies to take full advantage of these new switch features and characteristics, and the CSI is just one example. If successful, future IMD designs will benefit significantly from the advantages made possible by using WBG switches in the most suibtable converter topologies.

D. Drive Electronics Technology Advances and Future Directions

As important as the emerging WBG power device technology may be to achieve the long-term future vision of integrated motor drives, there is an equally urgent need for technology breakthroughs in many other aspects of the drive electronics in order to achieve the demanding objectives for power density and reliability/robustness in hostile thermal and vibration environments at an affordable cost. This section is devoted to providing a brief summary of some promising new technology developments that have been reported as well as remaining unmet needs. This discussion is broken into two major topics. The first topic addresses new technologies that primarily influence the long-term reliability and robustness of the IMD's drive electronics, and the second

topic focuses on technologies associated with achieving the goal of embedding the power electronics inside the motor enclosure.

1) Power Electronics Reliability/Robustness Technologies

Advanced Power Semiconductor Packaging: When working to take advantage of the extremely high switching frequencies and high junction operating temperatures of WBG power devices, it quickly becomes apparent that these advantages lose nearly all of their value unless the power semiconductor packages used to mount the WBG die and the associated power module packaging are completely compatible with these features. Unfortunately, the large majority of power device and module packages widely used today for silicon power devices are painfully deficient for use with WBG devices intended for use at either high switching frequencies (>100 kHz) or high junction temperatures (> 175 °C).

Focusing first on the issue of high-temperature operation and the related issue of thermal cycling with large temperature differences, there are a significant number of promising technologies that are either in development or already being introduced into the marketplace. Considering the typical power module cross-section layout illustrated in Fig. 23, the new technologies can be divided among those associated with making electrical connections to the die, and a second category associated with mounting the die on the substrate. TABLE II, which is not exhaustive, identifies a number of the new technologies that are designed to increase the power device's ability to operate at higher temperatures and withstand high thermal cycling.

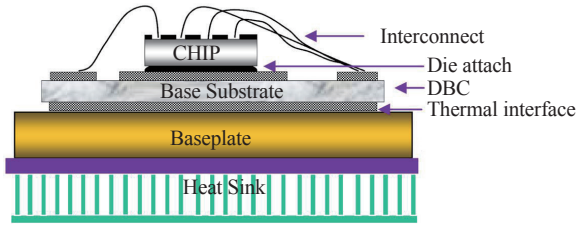


Fig. 23. Cross-section of conventional power module construction.

TABLE II
ADVANCED TECHNOLOGIES FOR POWER MODULE CONSRUCTION

Category	Solution Type	Representative Technologies	
Die Interconnect and Joining	Material	Sintered silver [60], MoCu [36], AlSiC [62]	
	Structure	Ribbon bonding [63], copper pin [64], solder ball [65], SKiN [66], Planar interconnect [67], Pressure contact [68]	
Substrate Construction	Material	Insulation layer	Al2O3 [61], AIN [69], LTCC [70]
		Conducting layer	DBA [60]
	Structure	Stepped edge [61]	

Recognizing the fatigue limitations of conventional wire bonds for electrical connections on the top-side of the power device die, there has been significant research and market introductions of alternative technologies that eliminate the wire bonds, often in favor of planar interconnect techniques. For example, the SKiN connection introduced by Semikron in 2011 offers a large thermal cycling reliability improvement compared to conventional wire-bond connections [66].

To minimize mechanical fatigue during high thermal cycling, sintered silver can be used as the die attach method in order to take advantage of its ability to absorb the repeated mechanical stresses associated with mismatches in the Coefficient of Thermal Expansion (CTE) between the die and substrate materials [60]. Some other materials (e.g., MoCu and AlSiC) offer a relatively close CTE match with SiC which helps to achieve more reliable die attachment. Another approach for improving the fatigue life of the die attach technique is based on modifying the die's geometric structure to provide better mechanical strength. As shown in [61], a die with stepped edges combined with a Al2O3 ceramic substrate exhibits more than 40x the thermal life cycle capability of normal die attachment to AIN direct-bond copper (DBC) substrates.

High-Temperature Passive Components and Controllers: In addition to improving the power module's high-temperature operation capabilities, other components of the IMD drive electronics including passive devices (capacitors and inductors) and control electronics also determine the maximum temperature limits of the unit.

Currently, high-temperature electronic components for motor drives is a niche market for special applications such as down-hole drilling and aerospace that demand it and can afford the significant cost premium. However, there is increasing interest in attaining higher-temperature operation for motor drives in other fields with larger markets such as automotive accessories and EV traction drives because of opportunities to save money by reducing/simplifying the cooling requirements [71]. New types of film capacitors are

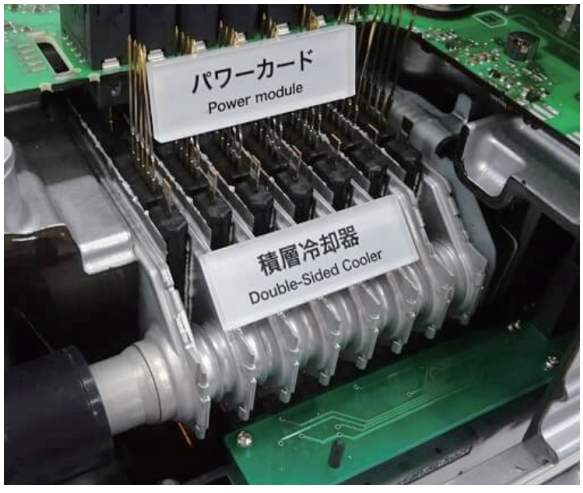


Fig. 24. Toyota EV traction inverter with double-sided cooling of power modules [79] used in Prius models.

being introduced that raise their maximum operating temperatures to 175 °C [72]. While some ceramic capacitors are already capable of operation at temperatures higher than 200 °C, new capacitor technologies based on alternative materials such as silicon [73] and glass [74] have been reported in the literature that can operate at temperatures greater than 250 °C and 200 °C, respectively. Inductor cores using powder as the core material are available that permit safe operation at temperatures up to 200 °C.

In addition to these passive components, integrated circuit technology is available that is compatible with high-temperature operation. For example, micro-controllers are already commercially available (albeit at a significant cost premium) with temperature ratings as high as 150 °C [75]. Turning attention back to the power electronics, researchers have successfully demonstrated high-temperature operation of a silicon-on-insulator-based gate drive operating in an ambient temperature as high as 200 °C [39].

Advanced Thermal Management: Taking advantage of continue advancement in additive manufacturing (3D printing) technology, complex shapes that are difficult or impossible to manufacture using traditional methods can be easily manufactured in a quick and cost-effective manner. For example, researchers at the UW-Madison [76] and Toyota [77] have demonstrated that they are able to build heatsinks with significantly higher thermal efficiency for both air and liquid cooling using additive manufacturing technology.

In addition to heatsinks, there has been effort to improve thermal dissipation by optimizing the thermal interface between the power devices and the heatsink. For example, there have been major research programs around the world working on reducing or eliminating the need for thermal interface materials that are designed to improve the thermal coupling between a power module's baseplate and the heatsink. One of the approaches that is already being used extensively by automotive manufacturers of EV inverters is direct substrate cooling technology [78].

In addition, Toyota was the first automotive manufacturer to introduce double-sided cooling of the power modules in the EV traction inverter for their 2008 Lexus hybrid LS600h model, and it more recently has been adopted for their hybrid Prius models (Fig. 24) [79]. Fig. 25 provides a visual summary of thermal cooling technologies adopted by various automotive manufacturers and suppliers during the past decade [80]. Other cooling methods under development for electronic assemblies with high thermal flux values include single-phase cooling, two-phase cooling, jet impingement and spray cooling, and thermoelectric cooling [81].

2) Advanced Power Converter Integration and Manufacturing Technologies

Conformal Power Electronics: As stated in Section IV.A, the long-term vision for integrated motor drives is to embed the drive electronics inside the motor enclosures. This is quite challenging since today's power electronics is generally predominantly two-dimensional, often using a flat printed circuit board as the skeleton for the power converter's

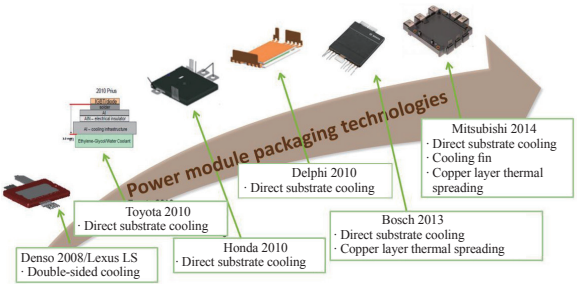


Fig. 25. Summary of advanced cooling technologies developed/adopted by automotive manufacturers and suppliers since 2008 [80].

physical design. The limitations imposed by this design and manufacturing paradigm for today's power electronics are quite restrictive when trying to convert this type of assembly into an embedded configuration that fits comfortably inside a motor enclosure with minimal modifications of the enclosure design.

One of the most promising pathways for escaping these limitations is additive manufacturing. An attractive feature of additive manufacturing is that it opens up the third dimension for the power electronic designer. This raises hope that additive manufacturing technology will eventually provide the key to developing drive electronics modules that can be conveniently designed to fit conformally within the contours of motor enclosures, such as inside the end bell assemblies. There are already some early reports of research efforts seeking to apply 3D printing technology to the fabrication of an inverter power stage, as shown in Fig. 26 [82]. However, the results presented to date suggest that this R&D is still in a very early stage, and there is much to be done to take full advantage of the possibilities made available by additive manufacturing technology.

As noted in the preceding discussion about advanced thermal management techniques, thermally-conductive polymers are being developed that can be used in the additive manufacturing process. This is intriguing in the context of future embedded IMD designs because it suggests that there

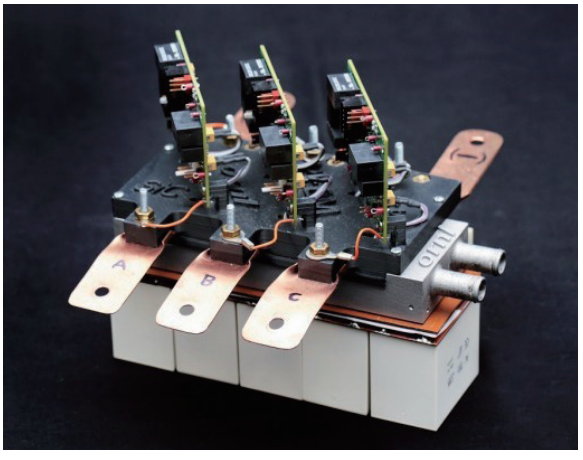


Fig. 26. Prototype 30 kW inverter with approx. 50% 3-D printed components [82].

might be clever techniques within reach for using these thermally-conductive structural materials to enhance the transfer of heat from the power electronics into the motor housing where it can be efficiently dissipated. Much more work is necessary to determine whether such concepts will lead to cost-effective approaches for manufacturing embedded power electronics in the future.

Higher Levels of Power Electronics Integration: The electronics for today's motor drives is generally manufactured using a large number of discrete parts that are mounted and interconnected using a printed circuit board. Even the gate drives are often custom-designed for each product using discrete parts, limiting the opportunities to drive down costs by manufacturing very large numbers of standardized commodity assemblies. The idea of power electronics integration is not a new one. For example, concept of Integrated Power Electronics Modules (IPEMs) was introduced in the late 1990s, integrating both active and passive components into compact assemblies [83]. This concept was later extended to higher-power applications using the Power Electronics Building Block (PEBB) concept [84]. Only some features of these approaches have gained wide acceptance by industry to date.

In 2002, International Rectifier introduced fully-integrated Intelligent Power Modules (IPMs) using silicon technology for special motor drive market segments including servo drives that integrated all of the power electronics including the inverter power state, gate drives, and all of the drive control electronics. Although these power modules provided impressive performance capabilities within a single EconoPack2 power module package, they did not succeed in the marketplace because of the economic challenges associated with gaining a sufficiently large production base to drive down the costs.

In summary, a combination of technology and economic hurdles has limited the development of a robust market for integrated motor drive electronics modules. Efforts are now under way to explore the opportunities that planar GaN technology may open for building inverters-on-a-chip using a monolithic integrated power electronics architecture [85]. Here again, time and patience will be required to determine how power electronics integration technology can play a role in driving down the cost of future IMDs with embedded drive electronics.

Power Electronics Modularization for Improved Manufacturability: As noted earlier in this paper when introducing the Integrated Modular Motor Drive (IMMD) technology in Section V.C, one of the motivations for the IMMD concept is to develop phase-drive units that include modularized power converters as a path to simplify manufacturing and drive down production costs. While there is significant evidence that modularization of power converters can work very effectively for static power supplies in applications such as data centers that require very large numbers of identical supplies, the evidence to prove the advantages of modularization in motor drives is much weaker to date. Depending on progress with the two preceding power electronics integration concepts in this section, it may be that drive electronics modularization will play a more important role in the future, but, for now, this topic remains primarily in the research realm.

VI. Conclusions

As indicated by its title, this paper has provided readers a summarized review of the past, present, and future of integrated motor drives. By highlighting key milestones in the history of IMDs stretching back more than 55 years, both the boldly innovative spirit of past generations of engineers who developed these landmark IMDs as well as the consistent progress towards higher levels of drive electronics integration and compactness have been very apparent. Taken together, this history points to a bright future for integrated motor drives as the drive electronics moves closer each year to complete absorption into the motor enclosure.

Of course, this ultimate objective cannot be achieved without multiple technology breakthroughs that will be required to enable such major progress. As discussed in this paper, there is reason for optimism that the necessary technology breakthroughs will appear and mature, leading to fulfillment of the vision of complete physical absorption that was noted above. Rapid development in the critical field of wide bandgap power semiconductors will be one of the most important technology contributors to achieving this future vision, but certainly not the only one.

A summary of key observations and conclusions to be drawn from this paper includes the following:

- Integrated motor drive technology has already left an indelible mark on the history of adjustable-speed drives as well as today's commercial motor drive offerings
- IMD technology will become significantly more powerful during coming years, culminating eventually in drive electronics that will be completely embedded in motor drive enclosures with little negative impact on the motor's mass or volume.
- Success in achieving this ambitious IMD vision will depend on the availability of future drive electronics that incorporates:
  - o New materials such as wide bandgap semiconductors and carbon nanotubes that will make it possible to significantly reduce the losses in the drive electronics and then remove the heat more effectively.
  - o New integration techniques that will make it possible and inexpensive to manufacture the drive electronics directly into the machine housing, escaping today's limitation that dictate primarily two-dimensional drive electronics.
  - o New concepts for achieving robustness/reliability objectives that will make it possible for all of the components in the drive electronics to operate for extended time periods in hostile thermal and vibration environments, accompanied by advanced diagnostics

and fault tolerance.

- The rate of progress towards achieving the long-term IMD vision depends heavily on taking a strongly multi-disciplinary, multi-physics approach to addressing the difficult technical challenges that must be overcome in order to achieve the vision.

The last point in this summary represents a serious challenge that calls for action by both industry and academia to nurture a new breed of engineers that is specially educated and trained to attack the most complicated cross-disciplinary technical problems that are retarding the future growth of IMD technology. Despite the tremendous progress that has been accomplished to date, achieving the full potential of integrated motor technology depends on a collective commitment to breaching the barriers between all of the engineering disciplines including electrical, mechanical, and materials in order to reach the ultimate limits of motor/drive integration. The rewards that will accompany success make overcoming these challenges well worth the effort.

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Advanced Control Strategies for Direct-Drive PMSG Wind Turbine Systems: Direct Predictive Torque Control Approaches

Zhenbin Zhang, José Rodríguez, and Ralph Kennel

***Abstract*—Full power scale back-to-back power converter PMSG wind turbine system, with direct-drive configuration, is an attractive solution, particularly for off-shore wind energy applications. For such systems, (nonlinear) direct control, which requires neither a modulation process nor cascaded linear controllers, but will operate the system at very high control dynamics, is a very promising control class. In this work, we reviewed and experimentally assessed the classical (C-), the duty-optimal (DO-), the ripple-reduced (RR-) and the multi-vector direct model predictive torque control (MV-DMPTC) solutions to deal with the generator side control of grid-tied full power scale back-to-back power converter PMSG wind turbine systems. Their theoretical background, realizations and control performances are presented and discussed. The realizations and experimental assessments of all the discussed control approaches are carried out with a fully FPGA based real-time controller, at a lab-constructed test-bench. The resource usage and implementation complexity are provided. Comprehensive evaluation results are given at the end.**

***Index Terms*—Direct torque control, FPGA, nonlinear control, predictive torque control, time optimal control, voltage source back-to-back power converters, wind turbine system with permanent magnet synchronous generator.**

I. Introduction

WIND energy installations have steadily increased over the last years.Wind turbine systems (WTSs) using fullscale back-to-back power converter and permanent-magnet synchronous generator (PMSG) with direct-drive configuration (without mechanical gear) are an interesting and promising alternative to doubly-fed induction generator based WTSs, due to its higher power density and more degrees of freedom in control and during grid faults. The electrical block diagram of a WTS with direct-drive PMSG and grid-tied back-to-back converter is shown in Fig. 1. Such a configuration allows for (see, e.g., [1]): (i) bidirectional power flow, (ii) an operation over a wide wind speed range, (iii) small DC-link capacitor volume and size, (iv) simple fault-ride through capabilities, and (v) reduced maintenance. These features make such WTSs attractive, in particular, for off-shore applications.

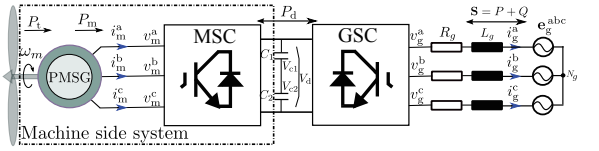

Fig. 1. A simplified structure of a grid-tied direct-drive back-to-back power converter PMSG wind turbine system, where $x_{g,m}$ are the variables for grid (g) and machine (m) side, $x \in \{i, e, v, R, L\}$ represents the current, grid and converter voltage (vector), resistance and inductance, respectively, V_d, ω_m, P, Q are the DC-link voltage and rotor speed, grid side active and reactive power, respectively. P_t and P_m is the power output of the wind turbine and generator, respectively. "MSC" and "GSC" represent "machine side converter" and "grid side converter".

Control schemes for the machine side convertor (MSC) of such systems (as shown in Fig. 1) can be divided into two classes (see, e.g., [2], [3]): (i) *(Linear) control schemes (with modulator) (e.g. with space vector modulation (SVM))*, such as (a) PI controller methods, e.g. field-oriented control (FOC) or (b) direct torque control (DTC) with modulator, and (c) deadbeat-like model predictive control (DBC) methods; and (ii) *(nonlinear) direct control schemes (without modulator)* such as (a) DTC with switching table (ST-DTC) and (b) (nonlinear) direct model predictive control (DMPC) approaches. From the concept point of view, the first class (partially) approximates the plant (i.e., the power converters and drives) as a linear and continues system, thereby, applying the "timed-average principle" with a modulator to emulate certain *continues* commands to the system. However, a switching power converter-fed energy conversion system is in essence a *nonlinear* and *switching-mode* plant. Modern digital controllers process a control algorithm in discrete format as well. Therefore, a more proper control philosophy shall be *nonlinear direct control*, which requires no *linear* and *continuous approximation*, but takes the nonlinear and switching-mode nature of the power converters and digital controllers into account *and* combines the modulation and switching sequence selection processes into *a single* step.

Switching table based direct control (*direct torque control* (ST-DTC) [4], [5] for machine side, and *direct power control* (ST-DPC) for grid side), which was originally developed in the 1980s for induction motor drives, has already been a very matured concept. In such solutions, the switching se-

Manuscript received August 20, 2017. This work was supported by DFG funding under Grant Nr.: KE817/32-1.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00020

quence are directly selected based on the mistake between the reference and the actual values with an offline designed switching table. No modulator or linear controller is required therein. Robust to parameter variations and very fast in control dynamics are their property. However, the switching table is *inflexible* (to deal with multiple control targets) and the control variable ripples highly depend on the *sampling frequency* of the system.

Recently, DMPC has been developed very fast in the field of power electronics and electrical drives. For such concept, instead of using a switching table, a very flexible *cost function* (also called the *objective function*) is utilized to define the control objectives and the full system model (including the power converter) is taken into account to determine an optimal control sequence. Similarly, no (complex) modulation process is required therein. Shortcoming, in the analogy to the ST-DTC approach, is that, the control variable ripples are very high in comparison with the classical modulator based solutions, due to that, only one switching vector will be selected and applied in a whole sampling interval.

To conquer this, many alternatives have been developed, e.g., the *duty-optimal* two-vector based direct predictive control (DO-DMPTC) method was proposed and presented in [6], [7], a *ripple-reduced* two vector direct model predictive torque control (RR-DMPTC) was proposed and reported in [8], [9], a *multi-vector* direct model predictive power control (MVDMPPC) was proposed and evaluated in [10], a *long-horizon* direct model predictive torque control (LH-DMPTC) was investigated in [11], [12], etc. Although LH-DMPTC results in a considerably improved control performances, in particular, at very low switching frequency cases, the required computational demands increase exponentially with the prediction horizon, and the key technologies to use such solution lie at the computationally intelligent methods to solve the so-called *nonlinear mixed-integer optimization problem* [12], [13], which goes beyond the scope of this work. On the other hand, the DO-, the RR-, and the MV-DMPTC remain still within the *short-horizon* direct model predictive control domain, invoking the so-called *time-optimal concept*. Simple modifications from the C-DMPTC will result in considerably improved control performances. Their slightly higher computational demands can be easily coped with by using field programmable gate array (FPGA) based real-time controller targets, which have already been a very popular solution (see e.g., [14]).

In this work, the C-, the DO-, the RR- and the MV-DMPTC control approaches for the machine side control of a two voltage level full-scale back-to-back power converter based PMSG wind turbine system are reviewed and comprehensively assessed. Both the controller designs and their theoretical backgrounds are discussed in detail. All methods are implemented on an FPGA-based real-time platform. Their control performances are compared experimentally with a labconstructed grid-tied PMSG wind energy system emulator.

This paper is organized as follows: In Sec. II, the machine side part of a grid-tied direct-drive back-to-back power converter PMSG wind turbine system is described and modeled in both continues- and discrete-time formats. In Sec. III, after revisiting the C-, the DO- and the RR-DMPTC solutions, we introduce a time-optimal MV-DMPTC approach. In Sec. IV, the FPGA design and measurement results are presented. At the end, Sec. V concludes this paper.

II. System Description and Modeling

In this section machine side system of a grid-tied full-scale back-to-back power converter PMSG wind turbine is described and modeled in *both* continues- *and* discrete-time formats to ease the understanding of the following controller design and analysis sections.

A. Continuous-Time Models

The dynamics of a PMSG are given by [13]

$$\left.\begin{aligned} \boldsymbol{v}_{\mathrm{m}}^{\mathrm{dq}} &= R_{\mathrm{s}}\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}} + \overbrace{\begin{bmatrix} L_{\mathrm{s}}^{\mathrm{d}} & 0 \\ 0 & L_{\mathrm{s}}^{\mathrm{q}} \end{bmatrix}}^{=:\boldsymbol{L}_{\mathrm{s}}^{\mathrm{dq}}} \frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}} + N_{\mathrm{p}}\omega_m \overbrace{\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}}^{=:\boldsymbol{J}} \boldsymbol{\psi}_{\mathrm{s}}^{\mathrm{dq}} \\ \boldsymbol{\psi}_{\mathrm{s}}^{\mathrm{dq}} &= \boldsymbol{L}_{\mathrm{s}}^{\mathrm{dq}}\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}} + \boldsymbol{\psi}_{\mathrm{pm}}^{\mathrm{dq}} \\ \tfrac{\mathrm{d}}{\mathrm{d}t}\omega_m &= \tfrac{1}{\Theta}\big[T_l - \underbrace{\big(N_{\mathrm{p}}(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}})^{\top}\boldsymbol{J}\boldsymbol{\psi}_{\mathrm{s}}^{\mathrm{dq}}\big)}_{=:T_e}\big] \end{aligned}\right\} \quad (1)$$

where $v_{\mathrm{m}}^{\mathrm{dq}} = (v_{\mathrm{m}}^{\mathrm{d}}, v_{\mathrm{m}}^{\mathrm{q}})^{\top}$, $i_{\mathrm{m}}^{\mathrm{dq}}=(i_{\mathrm{m}}^{\mathrm{d}}, i_{\mathrm{m}}^{\mathrm{q}})^{\top}$, R_{s}, $L_{\mathrm{s}}^{\mathrm{d}}$, $L_{\mathrm{s}}^{\mathrm{q}}$, N_{p}, ω_{m}, $\psi_{\mathrm{pm}}^{\mathrm{dq}} = (\psi_{\mathrm{pm}}, 0)^{\top}$, Θ, T_{e} and T_l are machine (applied) voltage and current vector, stator resistance, *d*-, *q*-stator inductances, number of pole pairs, machine angular velocity, permanent magnet flux linkage, inertia, electromagnetic torque and load torque, respectively. For two-level power converters, the admissible switching state u_{i} is within a finite set (See Fig. 2(a)), i.e.,

$$\boldsymbol{u}_{\mathrm{i}} \in \mathcal{U} := \{\boldsymbol{u}_0(000), \boldsymbol{u}_1(001), \cdots, \boldsymbol{u}_6(101), \boldsymbol{u}_7(111)\}. \quad (2)$$

Neglecting losses, the converter voltage vector in the *dq*-reference frame is calculated as [15]

$$\boldsymbol{v}_{\mathrm{m}}^{\mathrm{dq}}(\boldsymbol{u}_{\mathrm{i}}) = \mathbf{T}_{\mathrm{P}} \cdot \mathbf{T}_{\mathrm{C}} \cdot \underbrace{\frac{V_{\mathrm{d}}}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}}_{=:\boldsymbol{T}_{\mathrm{SW}}} \boldsymbol{u}_{\mathrm{i}}, \quad (3)$$

where $\mathrm{T_P}$ and $\mathrm{T_C}$ are the Park and Clark transformation matrices (See e.g., [13]), $\mathrm{V_d}$ is the DC-link voltage.

B. Discrete-Time Models

Defining the slope of $x(t)$ at sampling instant k as $g_x(k) = \frac{\mathrm{d}x(t)}{\mathrm{d}t}\Big|_{t=\mathrm{k}\cdot\mathrm{T_s}}$, where T_{s} is the sampling interval, and applying the Euler-Forward equation (i.e,$\frac{\mathrm{d}\vec{x}(t)}{\mathrm{d}t} \approx \frac{\vec{x}_{[\mathrm{k}+1]}-\vec{x}_{[\mathrm{k}]}}{T_{\mathrm{s}}}$) to (1),

yields the discrete-time slopes of the currents and electron-magnetic torque of the generator, at the drive force of switching vector u_i, as [13]

$$g_{i_m^d}^{\boldsymbol{u}_i}(k) = \frac{\mathrm{d}i_m^d(t)}{\mathrm{d}t}\Big|_{t=k\cdot T_s} = \frac{R_s}{L_s} i_m^d(k) + N_p\omega_m(k) i_m^q(k) + \frac{v_m^{d,\boldsymbol{u}_i}(k)}{L_s}, \quad (4a)$$

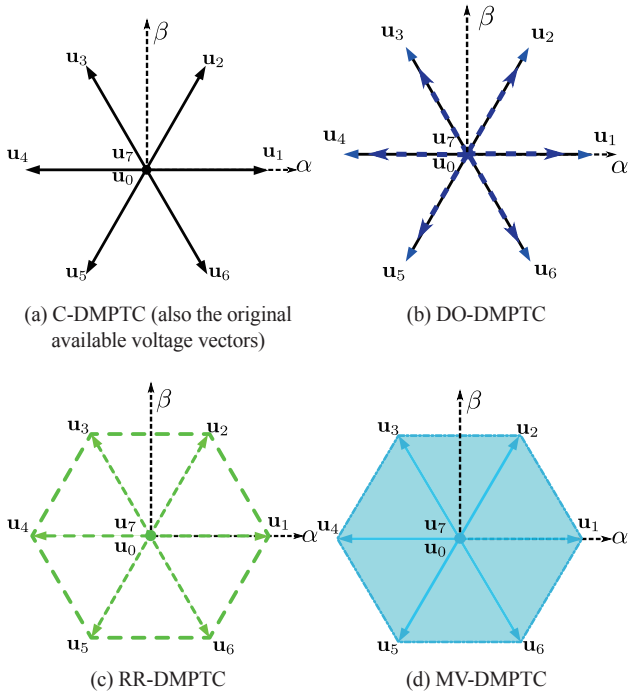
$$g_{i_m^q}^{\boldsymbol{u}_i}(k) = \frac{\mathrm{d}i_m^q(t)}{\mathrm{d}t}\Big|_{t=k\cdot T_s} = \frac{-R_s}{L_s} i_m^q(k) - N_p\omega_m(k) i_m^d(k) - N_p\omega_m(k)\frac{\psi_{pm}}{L_s} + \frac{v_m^{q,\boldsymbol{u}_i}(k)}{L_s}, \quad (4b)$$

$$g_{T_e}^{\boldsymbol{u}_i}(k) = \frac{\mathrm{d}T_e(t)}{\mathrm{d}t}\Big|_{t=k\cdot T_s} = N_p\psi_{pm}\cdot g_{i_m^q}^{\boldsymbol{u}_i}(k). \quad (4c)$$

The discrete models are useful to predict the future behaviors of the system, e.g., at $k+1$, at a drive force with vector u_i,

$$x(k+1) = x(k) + T_s \cdot g_x^{\boldsymbol{u}_i}(k), \quad (5)$$

where $x \in \{i_m^d, i_m^q, T_e\}$.



(a) C-DMPTC (also the original available voltage vectors) (b) DO-DMPTC

(c) RR-DMPTC (d) MV-DMPTC

Fig. 2. Candidate switching vector ranges/planes for the C-, the DO-, the RR- and the MV-DMPTC solutions.

III. Classical and Advanced Direct Predictive Torque Control Methods

For a grid-tied direct-drive PMSG wind turbine system, the inner loop control objectives of the machine (here the PMSG) side includes: (co_1) torque tracking with fast dynamics and accuracy (to meeting the outer maximum power point tracking), and (co_2) to achieve maximum efficiency and to best utilize the available stator currents, i.e., to meet the so-called maximum-torque-per-ampere (MTPA) requirements, and (co_3) the system shall operate within the allowed power range/constraint. Additionally, low torque/current ripples are desirable to reduce losses and mechanical bearing. Therefore a cost function of

$$J(\boldsymbol{u}_i) = \sum_{h=k}^{k+N-1} \Big(\underbrace{\left(T_e^* - T_e(k+1)(\boldsymbol{u}_i)\right)^2 + \gamma_{i_m^d}\left(i_m^d(k+1)(\boldsymbol{u}_i)\right)^2}_{=:J_{TS}} + J_{CS} \Big), \quad (6)$$

can be defined for a *surface-mounted* PMSG[1] to guarantee the above mentioned control objectives, where $h \in \mathbb{N}^+$ is the prediction horizon, $i \in \{0, 1, \ldots, 6, 7\}$ represents the number of the available switching vectors, J_{TS} represents the targets for torque and MTPA control.

$$J_{CS} = \gamma_I \cdot \mathrm{if}\{\|\boldsymbol{i}_m^{dq}(k+1)\| > \|\boldsymbol{I}_m\|^{max}\} \quad (7)$$

represents the limitation constraint of the system, where $\|I_m\|^{max}$ is the system permissible current limit, $\gamma_I (> 0)$ is the weighting factor[2]. In this work, a "one-step" prediction is considered for a fair comparison.

In the following, within the nonlinear direct control class, the classical direct model predictive torque control (i.e., the C-DMPTC), and three recently reported more advanced direct model predictive torque control solutions (i.e., the DO-, the RR- and the MV-DMPTC) are presented. Note that, the outer speed controller (here the same proportional integration (PI) controller as in [16], [17] is adopted) is not the scope of this paper and is therefore not redundantly reported.

A. Classical DMPTC (C-DMPTC)

The C-DMPTC scheme [13] evaluates the given cost function (6) for all the admissible (finite) set $\mathcal{U}$ (see (2)) by using the prediction model presented in (5), i.e.,

$$(\boldsymbol{u}_x^\star, \boldsymbol{t}_x^\star) := \arg\min_{x\in\{0,\ldots,7\}} J(\boldsymbol{u}_i)\Big(\boldsymbol{i}_m^{dq}(k+1), T_e(k+1)\Big), \quad (8)$$

However, the optimal vector $u_x^\star$ in this case can only be one of the original eight fundamental vectors, i.e., one of the black lines or the origin in Fig. 2(a), and will be applied for a whole control interval (so $t_x^\star := T_s$), i.e., "one-vector-per-control-interval". Therefore, when the ideal equivalent voltage vector (which could "zerolize" the difference between the reference and the real value) is far away from these fundamental vectors, a rough approximation will lead to big control variable ripples during the steady state. Inspired by this, a duty-opt direct model predictive control method (i.e., the DO-DMPTC) was firstly proposed in [6], [7]. In the following, it will be detailed.

[1] In this work a surface-mounted PMSG was used, i.e., $L_s^d \approx L_s^q$. Therefore, $i_m^{d*} := 0$ will lead to the so-called MTPA control, for which, the detailed analysis can be found in e.g., [13].

[2] Note that, for both the DO- and RR-DMPTC methods to be introduced in the following, γs in (6) is set to be zero (i.e., the constraint is not considered) so that the cost function becomes (globally) differentiable, and the duty cycles can be calculated.

B. Duty-Optimal DMPTC (DO-DMPTC)

In the concept of the DO-DMPTC, instead of "one-vector-per-control-interval", two vectors, i.e., *one active* and *one zero* vector, are chosen to minimize the cost-function. Detailed realizations are as follows: Inserting (5) into the targeting set of (6) and invoking the time-optimal concept [10], [14], i.e.,

$$\begin{aligned} &\frac{\mathrm{d}J_{\mathbf{TS}}(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}}(k+1), T_{\mathrm{e}}(k+1), (\boldsymbol{u}_{\mathrm{x}}^{\star}, \boldsymbol{u}_{\mathrm{y}}^{\star}))}{\mathrm{d}\boldsymbol{t}_{\mathrm{x}}^{\star}} \stackrel{!}{=} 0, \\ &\text{s.t.}: \quad \boldsymbol{t}_{\mathrm{x}}^{\star} + \boldsymbol{t}_{\mathrm{y}}^{\star} = T_{\mathrm{s}} \end{aligned} \tag{9}$$

for all the six neighboring vector pairs[3]. Then through the following optimization process of

$$\begin{aligned} &(\boldsymbol{u}_{\mathrm{x}}^{\star}, \boldsymbol{t}_{\mathrm{x}}^{\star}, \boldsymbol{u}_{\mathrm{y}}^{\star}, \boldsymbol{t}_{\mathrm{y}}^{\star}) := \\ &\arg\min_{x\in\{1,\cdots,6\}, y\in\{0,7\}} J_{\mathbf{TS}}\Big(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}}(k+1), T_{\mathrm{e}}(k+1)\Big), \end{aligned} \tag{10}$$

The final solutions of $u_{\mathrm{x}}^{\star}$, $t_{\mathrm{x}}^{\star}$, $u_{\mathrm{y}}^{\star}$ and $t_{\mathrm{y}}^{\star}$ will be obtained. In the up coming interval, the switching vectors of $u_{\mathrm{x}}^{\star}$ and $u_{\mathrm{y}}^{\star}$ will be applied with their time durations of $t_{\mathrm{x}}^{\star}$, $t_{\mathrm{y}}^{\star}$, respectively. Such process in essence results in that, an equivalent vector of u^{DO}, in phase with the selected active vector, with an *optimized length* can be synthesized, i.e., the available candidate switching vectors have been greatly extended to *arbitrary lengths* at the phases of all the *original active switching vectors* (See Fig. 2(b)). Therefore, better steady state performance than the C-DMPTC can be achieved. However, an equivalent vector with phases (directions) other than that of the *fundamental* active vector cannot be synthesized; the performance improvement is hence still limited.

C. Ripple-Reduced DMPTC (RR-DMPTC)

Inspired by the analysis above, a so-called "ripple reduced direct model predictive control" (RR-DMPC) scheme was proposed to further enhance the system performance [8], [13]. Different from both the C- and the DO-DMPTC schemes, with the RR-DMPC, an equivalent vector, is still synthesized with two vectors. However, instead of only one active and one zero vector, any of the neighboring vector pairs, including the two active ones are also used. To realize RR-DMPTC concept, again, the time-optimal concept will be applied, considering both the vector pairs of two active ones, and one active with one zero vectors. In the analogy, through the following optimization process of

$$\begin{aligned} &(\boldsymbol{u}_{\mathrm{x}}^{\star}, \boldsymbol{t}_{\mathrm{x}}^{\star}, \boldsymbol{u}_{\mathrm{y}}^{\star}, \boldsymbol{t}_{\mathrm{y}}^{\star}) := \\ &\arg\min_{x\in\{1,\cdots,6\}, y\in\{0,\cdots,7\}} J_{\mathbf{TS}}\Big(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}}(k+1), T_{\mathrm{e}}(k+1)\Big), \end{aligned} \tag{11}$$

[3]Note that, for all the DO-, RR- and MV-DMPTC solutions, u_{x}, u_{y} are geometrical neighbors, following the relationship shown in Fig. 2(a), e.g., if u_{x} is (000), then u_{y} will be (001), if u_{x} is (001), u_{y} will be (011). This way will reduce both the computational efforts and switching transitions.

The optimal switching vectors with their operating time durations will be obtained and applied. Note that, u_{y} in this case includes also the active neighbors of u_{x}. With such process, both optimized "phase" (at a full length, reaching the boundary of the hexagon plane) and an arbitrary length (at all the original active vector phases) are now available (see Fig. 2(c)). Easy to understand, better performances than both the C-DMPTC and DO-DMPTC are expected.

D. Multiple-Vector DMPTC (MV-DMPTC)

Although both the DO- and RR-DMPTC have extended the available candidate vector range, the entire potential of a power converters operation range, i.e, the whole hexagon plane, however, remains to be fully explored. Meanwhile, the undifferentiable constraint (e.g., system operation limits) was not included into the cost function. In [10], [13], a multiple vector direct model predictive power control (MV-DMPPC) scheme, which will utilize maximally three vectors, was presented to deal with the grid side control of the wind energy systems. Such scheme has fully utilized the whole plane of the hexagon, but still combines the optimization and modulation stages within one single process. The concept, when applied to the machine side with torque control, i.e., MV-DMPTC, will go through the following three steps:

1) *Optimal direction detection:* Ease to understand, only grouping an active pair will synthesize a new vector with different directions (other than any of the original active pair). In this step, all the neighboring active vector pairs will be selected. Again the time-optimal concept will be used to obtain their duration times. I.e., applying (14) for all the six neighboring vector pairs, and invoking again the minimization process of

$$\begin{aligned} &(\boldsymbol{u}_{\mathrm{x}}^{\star}, \boldsymbol{t}_{\mathrm{x}}^{\star}, \boldsymbol{u}_{\mathrm{y}}^{\star}, \boldsymbol{t}_{\mathrm{y}}^{\star}) := \\ &\arg\min_{x\in\{1,\ldots,6\}, y\in\{1,\ldots,6\}} J_{\mathbf{TS}}\Big(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}}(k+1), T_{\mathrm{e}}(k+1)\Big), \end{aligned} \tag{12}$$

will lead to a single optimal pair of vectors, with which, through the following equation of

$$\boldsymbol{u}_{\mathrm{new}}^{\star} := \frac{\boldsymbol{t}_{\mathrm{x}}^{\star}}{T_s} \cdot \boldsymbol{u}_{\mathrm{x}}^{\star} + \frac{\boldsymbol{t}_{\mathrm{y}}^{\star}}{T_s} \cdot \boldsymbol{u}_{\mathrm{y}}^{\star}. \tag{13}$$

a vector with a new direction will be obtained. This vector will be used in the following step to further tune its length, in combination with a zero vector.

2) *Optimal vector length detection:* Less ideally, the length of the above obtained new vector of $u_{\mathrm{new}}^{\star}$ shall be tuned again, so an optimal vector can be obtain to achieve good steady state control performances. In this case, a zero vector shall be combined again with $u_{\mathrm{new}}^{\star}$. This process requires again the time optimal concept, i.e.,

$$\begin{aligned} &\frac{\mathrm{d}J_{\mathbf{TS}}(\boldsymbol{i}_{\mathrm{m}}^{\mathrm{dq}}(k+1), T_{\mathrm{e}}(k+1), (\boldsymbol{u}_{\mathrm{new}}^{\star}, \boldsymbol{u}_{\mathrm{null}}^{\star}))}{\mathrm{d}\boldsymbol{t}_{\mathrm{new}}^{\star}} \stackrel{!}{=} 0, \\ &\text{s.t.}: \quad \boldsymbol{t}_{\mathrm{new}}^{\star} + \boldsymbol{t}_{\mathrm{null}}^{\star} = T_{\mathrm{s}}, \ \mathrm{null} \in \{0, 7\}. \end{aligned} \tag{14}$$

At the end, the final duration times of the above vectors (u_x, u_y, u_{null}) will be obtained by

$$\boldsymbol{t}_{\mathrm{x}}^{\mathrm{opt}} = m \cdot \boldsymbol{t}_{\mathrm{x}}^{\star}, \tag{15a}$$
$$\boldsymbol{t}_{\mathrm{y}}^{\mathrm{opt}} = m \cdot \boldsymbol{t}_{\mathrm{y}}^{\star}, \tag{15b}$$
$$\boldsymbol{t}_{\mathrm{null}}^{\star} = T_{\mathrm{s}} - \boldsymbol{t}_{\mathrm{x}}^{\mathrm{opt}} - \boldsymbol{t}_{\mathrm{y}}^{\mathrm{opt}}, \tag{15c}$$

where $m := \frac{\boldsymbol{t}_{\mathrm{new}}^{\star}}{T_{\mathrm{s}}} \in [0, 1]$.

3) *Constraint inclusion:* Not difficult to understand, the constraint violence happens when the current limit has already been reached but the reference tracking is still not met. A deep analysis for this situation will yield that, since the length of the vector obtained after Step D-1) can be tuned down to zero in Step D-2), only an improper direction/phase (i.e., direction optimization process in Step D-1) is improper) will lead to such violence. Inspired by this, a solution to include the system constraint by adding a comparison step, invoking the predictive constraint term in (6), after the aforementioned two steps, so to respect the whole cost function more properly.

IV. FPGA Design

The use of Field Programmable Gate Arrays (FPGAs) as part of the control platform in power electronics and electrical drive systems has been reported in both academic and industrial applications [18], [19]. In this work, all the algorithms (including C-, the DO-, the RR- and the MV-DMPTC) are divided into sub-routines and implemented invoking the Single-Cycle-Timed-Loop (SCTL) technique on an entirely FPGA based platform. Due to the limited space, only the overall FPGA design structure for the MV-DMPTC is given in Fig. 3.

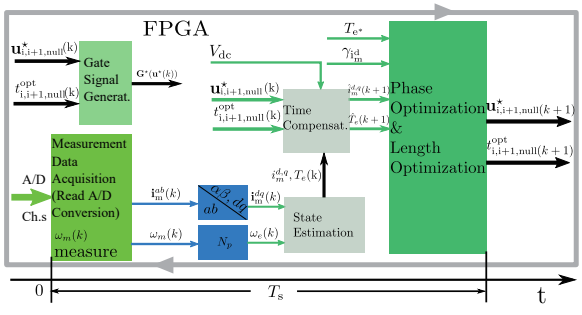


Fig. 3. FPGA design of the proposed MV-DMPTC control scheme (note that, to keep the scope, the speed and MPPT control loops are not presented in this figure. The time compensation part is the same as presented in e.g., [8], [10]).

[4]The top clock is 40MHz, therefore, 1[tick] = 1/40000000[s]

[5]These data show the FPGA resource usage of the four schemes (solely for the grid side control). The resource cost for commutation interfaces, data acquisitions, signal saving blocks, etc. was not taken into account. Primary code optimizations are considered to save some resources, in particular for the last three methods (i.e., the DO-, RR- and MV-DMPTC), during their FPGA realizations.

The overall comparison during the FPGA program implementation is presented in TABLE I. As can be seen, higher resource usage is seen with the more advanced direct control approaches.

TABLE I
FPGA Design Overall Comparison

	Calculation Time[4]	Resource Usage[5]
C-DMPTC:	169[ticks]	19%
DO-DMPTC:	217[ticks]	28%
RR-DMPTC:	278[ticks]	32%
MV-DMPTC:	524[ticks]	38%

V. Effectiveness Evaluation and Analysis

In this section the effectiveness evaluations of all the aforementioned approaches were compared with *both* simulation *and* experimental data. The system configuration and parameters are collected in TABLE II.

TABLE II
System Parameters

Parameters	Values
Generator stator inductance L_s [H]	$8{\cdot}10^{-3}$
Generator stator resistance R_s [Ohm]	1.3
Generator nominal torque / current T_e^n /I_m^n [Nm/A]	7.5/5
Permanent-magnet flux ψ_{pm} [Wb]	0.41
Generator pole pair number N_p [1]	3
Grid (phase) voltage e_g^a [V] (peak)	120
Grid frequency ω_g [rad/s]	100π
Grid side resistance R_g [Ohm]	$1.56{\cdot}10^{-3}$
Grid side inductance L_g [H]	$16{\cdot}10^{-3}$
DC-link capacitance C:= C_1+C_2 [μF]	1100

A. Simulation Verification

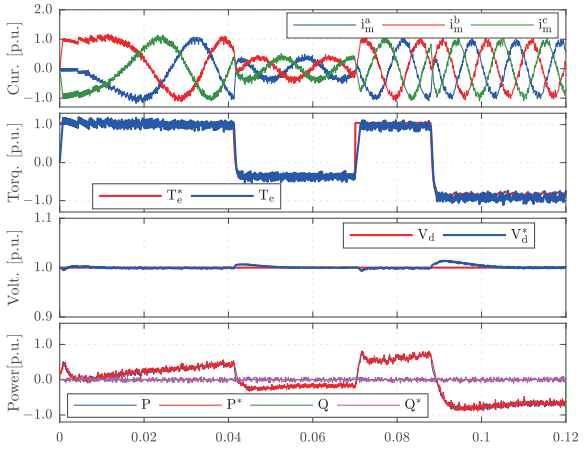
The overall control performance comparison among the C-, the DO-, the RR- and the MV-DMPTC methods are carried out through Matlab/Simulink as a preliminary concept of proof. The simulation results are shown in Fig. 4, where the same outer control loop and test situations are configured for all these four methods for a fair comparison. As can be seen, control dynamics remain almost the same, while greatly reduced steady state control variable ripples are seen with all the DO-, the RR- and the MV-DMPTC control solutions, with the MV-DMPTC being the best solution among the afore-discussed approaches.

To illustrate the detailed steady state control performances and to better understand the background forces for the steady state current/torque performances, a steady state control performances are shown in Fig. 5. As can be seen, at the same sampling frequency, the best current quality is achieved with the MV-DMPTC solutions, where the estimated synthesized voltage vector of $\hat{v}_m^*$ (estimated with the switching vector)

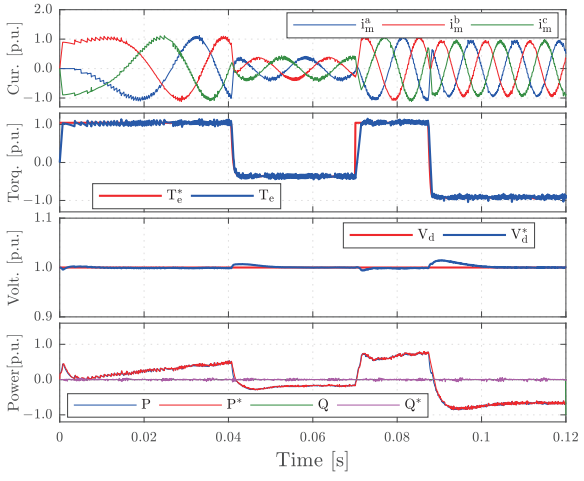
shows the most smooth waveform. These voltage vectors at a large extend determines the steady state performances of a switching power converter driven system.

B. Experimental Verification

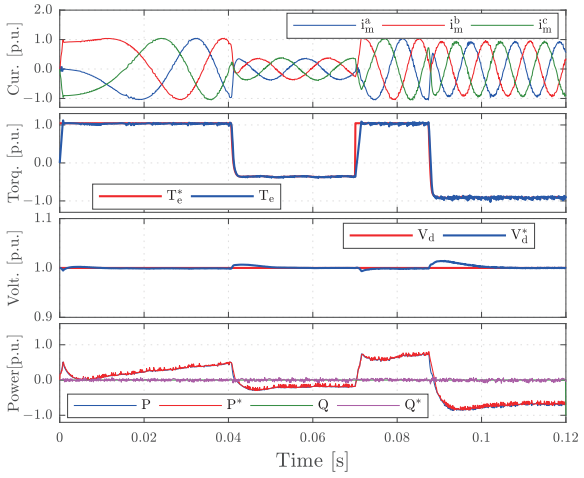
To experimentally evaluate the proposed scheme, a Lab-



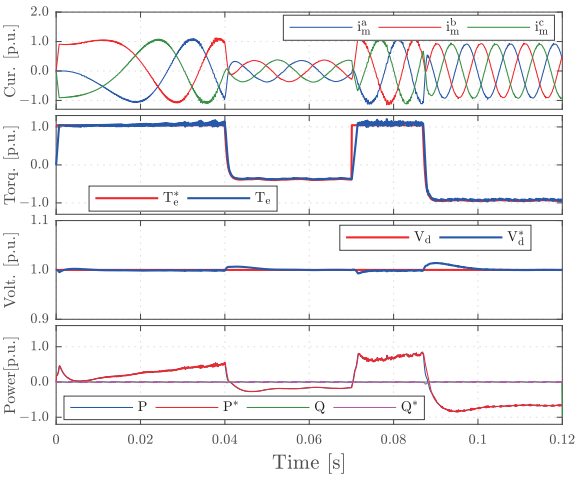
(a) C-DMPTC



(b) DO-DMPTC

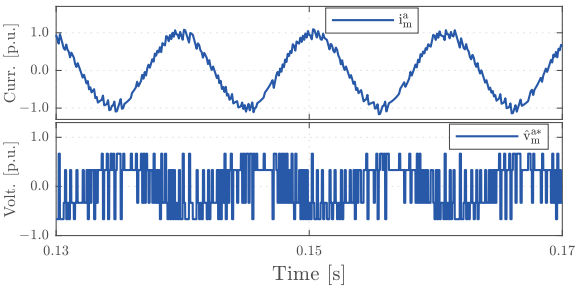


(c) RR-DMPTC

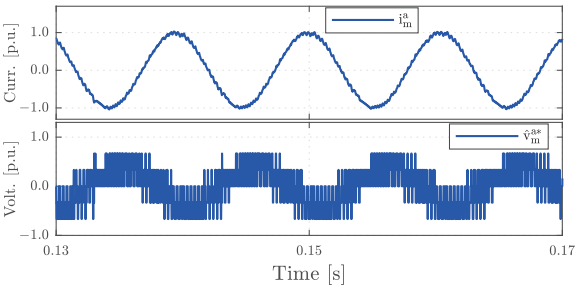


(d) MV-DMPC

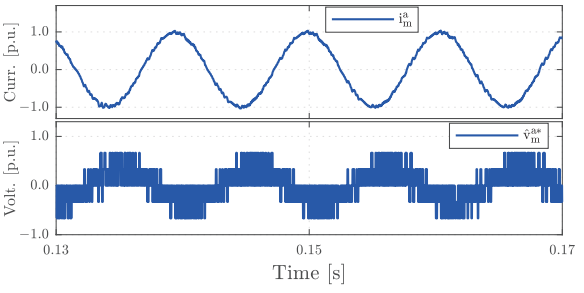
Fig. 4. [Simulation data:] Overall control performance comparison. For each figure, from up to down are: the stator currents, electromagnetic torque, DC-link voltage, grid side power, grid side phase voltage and current, respectively, all in p.u. values.



(a) C-DMPTC

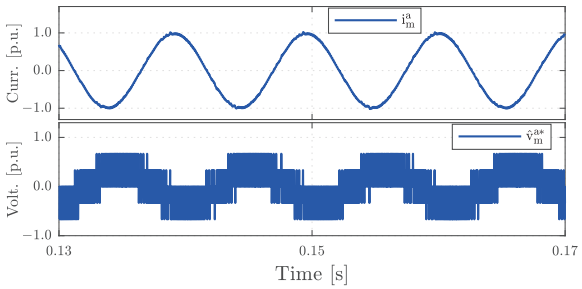


(b) DO-DMPTC



(c) RR-DMPTC

Fig. 5. [Simulation data:] Steady state control performances. For each figure, from up to down are: the generator stator currents and generator side converter (estimated) commanded voltages; grid side current and grid side converter (estimated) voltage, respectively.



(d) MV-DMPTC

Fig. 5. *(Continued.)* [Simulation data:] Steady state control performances. For each figure, from up to down are: the generator stator currents and generator side converter (estimated) commanded voltages; grid side current and grid side converter (estimated) voltage, respectively.

prototype of a grid-connected PMSG wind turbine system with full scale back-to-back power converter and grid side (R)L-filter has been constructed. The laboratory prototype is depicted in Fig. 6. A variac is installed between grid and choke (RL-filter) to step down the grid side voltage for safety reasons. A fully FPGA based reconfigurable real-time system (NI-cRIO system) is used to implement all the discussed predictive controllers. The measurement results are shown in Fig. 7. As expected, considerably improved performances, in terms of smaller torque and current ripples and THD values, are seen in particularly with the RR- and MV-DMPTC solutions.

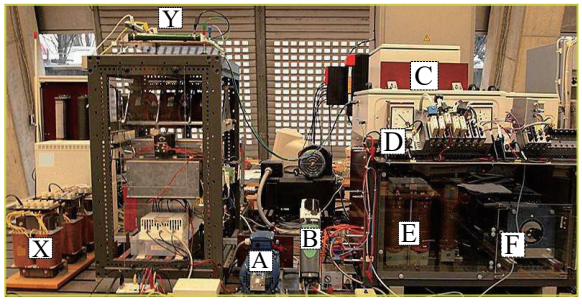
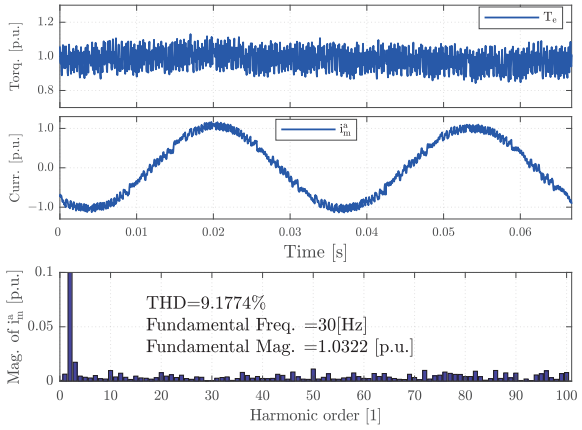


Fig. 6. Laboratory setup of a *grid-connected back-to-back converter with PMSG* with (A) turbine emulator (AC-Motor) and PMSG, (B) load motor drive, (C) back-to-back voltage source converter (constructed using Infineon IGBT modules), (D) NI-cRIO FPGA based controller, (E) grid-side choke (inductance L_g with resistance R_g) and (F) grid-side variac, (X) and (Y) are the passive load for testing in islanding mode.

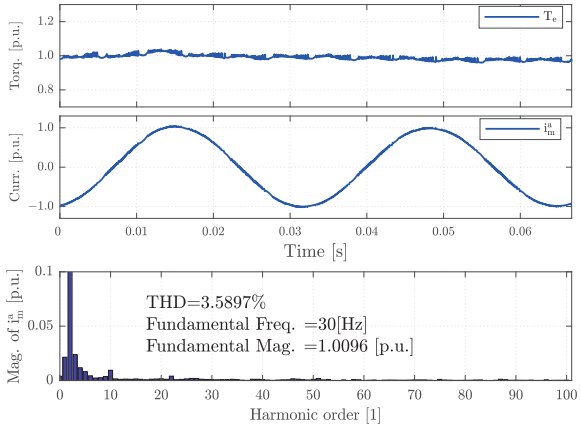
C. Discussion

In deep view of any control method for a switching power con-verter based system (including both the modulator and non-modulator based techniques) will yield such a conclusion: for all the available methods, forces to fulfill the control objectives are no more than *three* types, i.e., *the admissible vector slopes during one control interval, duration time of each slope* and *their actuating arrangement* (i.e., the pulse pattern). Considering only the first two, we can category the four direct model predictive control methods discussed in this paper with TABLE III.

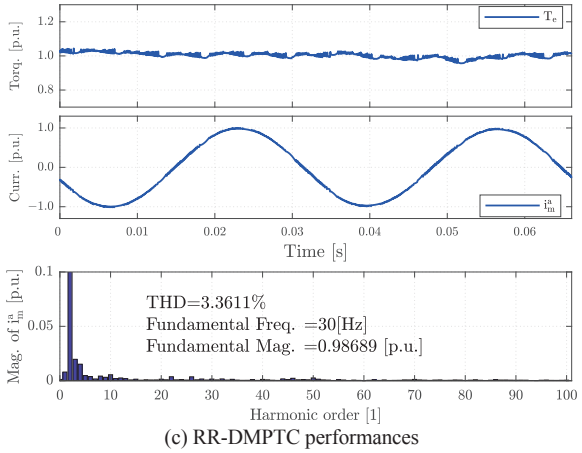
As can be seen from TABLE III, both the vector slopes and their actuating times can be optimized with the MV-DMPTC solution, therefore, best control performances are expected using such solution, in comparison with the C-, the DO- and the RR-DMPTC methods.



(a) C-DMPTC performances

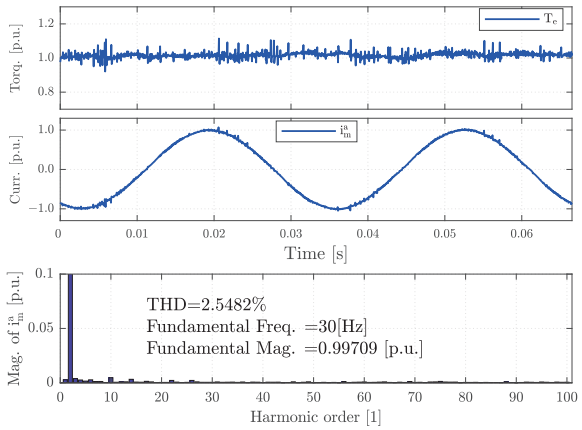


(b) DO-DMPTC performances



(c) RR-DMPTC performances

Fig. 7. [Experimental results:] Performances of the C-, the DO-, the RR- and the MV-DMPTC methods. From up to down are the machine electromagnetic torque, the stator phase current and the current spectrum, respectively.



(d) MV-DMPTC performances

Fig. 7. *(Continued.)* [Experimental results:] Performances of the C-, the DO-, the RR- and the MV-DMPTC methods. From up to down are the machine electromagnetic torque, the stator phase current and the current spectrum, respectively.

TABLE III
PROPERTIES OF THE FOUR DIRECT MODEL PREDICTIVE CONTROL SCHEMES

Methods	Vector slopes	Actuating time
C-DMPTC	Fixed and limited	Fixed (= T_s)
DO-DMPTC	Fixed and limited	Unlimited, partially optimized
RR-DMPTC	Unlimited and optimized	Unlimited, partially optimized
MV-DMPTC	Unlimited and optimized	Unlimited, optimized

VI. CONCLUSION

As a promising nonlinear direct control class, *direct model predictive control* has already become a viable alternative for both grid-tied active front end and machine side power converter control of wind turbine systems. However, the inherent one-vector-per-control-interval character of the classical DMPTC leads to relatively big control variable ripples, in particular for the two-level cases. This makes the investigation on steady state performance enhanced approaches quite necessary. Following such requirement, the DO-, the RR- and the MV-DMPTC solutions have been investigated and discussed comprehensively in this paper. The former two solutions utilize (maximum) two vectors (which can be two active ones or one active and one zero vector), and extend the candidate synthesized vector range to another freedom: phases (directions) other than the fundamental active ones; The latter (MV-DMPTC), by using (maximally) three vectors, makes the whole hexagon plane reachable.

Although the DO-, the RR- and the MV-DMPTC solutions have improved the control performances very considerably, both the required computational efforts and switching frequencies are higher than those for the C-DMPTC solution. However, looking into the future, increasing advanced embedded/real-time hardware (e.g., FPGAs) and the new power electronic devices (e.g., SiC devices) have already been accessible, the computational demands and high switching frequency requirements will not be a problem.

ACKNOWLEDGEMENTS

This research was made possible by the hardware support of National Instruments and Infineon. Dr.-Ing. Zhenbin Zhang would like to express his gratefulness to Dr.-Ing Martin Schulz (from Infineon); Mr. Marc Backmeyer, Mr. Zwick Wolfgang, Mr. Jan Kniewasser (from NI, Germany) and Mr. Dietmar Schuster (from EAL of TUM) for their help during the test-bench construction.

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A Survey on Space-Vector Pulse Width Modulation for Multilevel Inverters

Qamar Muhammad Attique, Yongdong Li, and Kui Wang

***Abstract*—The selection of an appropriate modulation scheme plays a vital role to assure the performance of multilevel inverters. Space vector pulse width modulation (SVPWM) is more efficient among all other pulse width modulation (PWM) techniques due to its key characteristics like better DC voltage utilization, switching losses reduction and easiness in digital implementation. The conventional SVPWM scheme presents some computational complexities due to redundant switching states and large number of space vectors. This paper summarizes five different SVPWM techniques for multilevel inverters which are *α-β* frame, *g-h* frame, *K-L* frame, *α′-β′* frame and SVPWM based on imaginary coordinate system. *g-h* frame and *K-L* frame are based on 60° and 120° coordinates system respectively. To compare the result of these SVPWM schemes, the complex calculations of conventional SVPWM are converted into simplified line voltages form. The comparison results validate all the SVPWM techniques, but the SVPWM based on imaginary coordinate is found more simple in duty ratio calculations, easier to understand and provides a better control for zero-sequence component for any level of inverter.**

***Index Terms*—g-h frame, imaginary coordinate system, *K-L* frame, multilevel inverters, space vector pulse width modulation (SVPWM), *α′-β′* frame.**

I. Introduction

NOWADAYS, the extensive use of multilevel inverters in high power and high voltage applications has made it a point of attraction for the researchers because of their remarkable performance. As compared with two-level inverters, multilevel inverters have various advantages, e.g. less harmonics in output current and voltages, reduced voltage stress across switching devices, lower dv/dt, better output wave form quality and lower common mode voltages [1], [2]. The diode-clamped 3 level neutral-point clamped (NPC) topology, as shown in Fig. 1 has been the most widely used one among all multilevel inverter topologies that have been proposed in literature [3]-[5].

By using an appropriate PWM technique, from discrete voltage levels, multilevel inverters generate the sinusoidal output voltages of different frequencies. Multilevel inverter's output performance depends on modulation algorithm and various PWM algorithms have been developed so far to fulfill the following objectives: less total harmonic distortion (THD), wider linear modulation range, lower switching losses and easy implementation. Among these, the two most popular PWM generation algorithms for multilevel inverters are sinusoidal carrier-based PWM (SPWM) and space vector PWM (SVPWM). In engineering applications, SPWM algorithms maintained their credibility for a long period [6]-[10] but with the development of microcontrollers, SVPWM took place due to its easy digital implementation, better harmonics performance, high DC voltage utilization ratio, reduced switching losses and convenience for capacitor voltage balancing. Moreover, the SVPWM has 15% higher linear modulation range than that of SPWM [11]. However, by increasing the number of levels, SVPWM faces the problem of more complex computations as compared to carrier-based PWM. Therefor many efforts have been made to achieve the SVPWM's performance by using zero-sequence voltage injection in carrier-based PWM [12]-[16]. Relationship between space vector and phase disposition carrier modulation is presented in [17] for hybrid and diode clamped multilevel inverters.

Any N-level inverter consists of six sectors and N^3 switching states in its space vector (SV) diagram while each sector comprises on $(N-1)^2$ triangles. There are $1 + s\sum_{i=1}^{N-1} i$ (here S is the total number of sectors and N shows number of level) switching vectors having one or more switching states that depends on its location in space vector diagram. The switching states with equal line to line voltages are known as redundant states in SV diagram. By choosing an optimal switching sequence of these states, certain objectives can be accomplished such as: common-mode voltage reduction [18]-[20], extension of modulation index [21], fault tolerance operation [22], switching frequency reduction [20], [23] and balancing of DC link capacitor voltages [18], [24]-[27]. Voltage balancing of DC-link capacitors in NPC converters is one of the essential problems that causes the deviation of output voltages from the reference value, also damage the equipment and devices [28]-[33]. If the sinusoidal PWM algorithm is used, the control of neutral point voltage is done by injecting the appropriate zero-sequence voltage in the reference voltage [34]-[37]. A relation between zero-sequence voltage and neutral current for NPC three-level converters is presented in [38].

By increasing the level of inverter, number of switching states and triangles becomes quite large which causes complexities in on-time calculations of switching periods. For example, the space vector diagram for three-level inverter has 27 switching states and 24 triangles while five-level inverter has 125 switching states and 96 triangles. So, the traditional SVPWM algorithms [39], [40] by using trigonometric function calculations becomes impractical as level of inverters increases. So far, various SVPWM algorithms have been presented in literature [41]-

Manuscript received September 9, 2017.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00021

[51] to diminish the problem of computational complexities.

A decomposition method was introduced in [41] and also implemented in [42], [43], by which the SV hexagon of three-level inverter is decomposed into six two-level SV hexagons. This method still has huge complications for increased level. For five-level inverter, SV diagram should be decomposed into six hexagons of four-level and then each four-level hexagon should be decomposed into six hexagons of three-level and so on. A fast SVPWM algorithm based on 60° coordinate system has been presented in [44] but does not consider proper switching states sequence and capacitor voltage balancing. Another effort has been made in [47] by proposing a general SVPWM algorithm based on imaginary coordinate system including the control of zero-sequence component. Two different non-orthogonal SVPWM strategies have been implemented in [48] and [51].

This paper summarizes the five different SVPWM algorithms for multilevel inverters which are α-β frame, *g*-*h* frame, *K*-*L* frame, α'-β' frame and SVPWM based on imaginary coordinate system. The complex calculations of conventional SVPWM are converted into simplified line voltages form and the results are compared for all aforementioned algorithms. The comparison results validate all the SVPWM techniques, but the SVPWM based on imaginary coordinate is more simple in duty ratio calculations, easier to understand and provides a better control for zero-sequence component for any level of inverter.

II. The Conventional (α-β Frame) SVPWM Algorithm

The basic diagram of 3-level diode-clamped inverter is shown in Fig. 1 which contains twelve switching devices (four in each leg) and three output levels for each phase (2, 1, 0). The relation between these devices and output level of each leg is shown in TABLE I. Fig. 2 shows the space vector diagram of three level inverter which consists of 24 active voltage vectors (6 large vectors, 6 medium vectors, 12 small vectors) and three zero vectors (222, 111, 000). SV diagram is divided in to six sectors (labeled as sector I to VI), each sector is divided into four triangles (labeled as triangle 1 to 4), 24 triangles in total. The implementation of space vector PWM comprises of the sector identification where the reference voltage vector is located, identification of three nearest switching vectors, selection of an appropriate switching sequence and on-time calculation of switches for specific switching sequence.

The reference vector V_{ref} corresponding to the three-phase

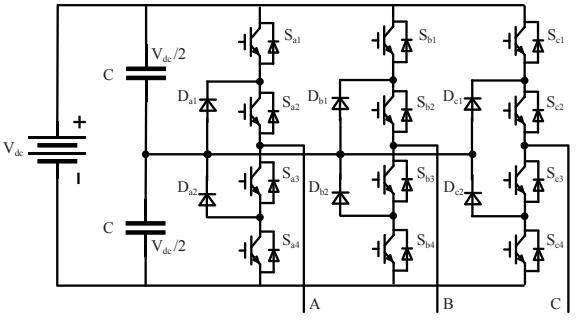

Fig. 1. Three level diode clamped NPC inverter.

TABLE I
Relationship Between Switching Devices and Output Level

ON Devices	OFF Devices	Output Level	Terminal Voltage
S_{x1}, S_{x2}	S_{x3}, S_{x4}	2	$+V_{dc}/2$
S_{x2}, S_{x3}	S_{x1}, S_{x4}	1	0
S_{x3}, S_{x4}	S_{x1}, S_{x2}	0	$-V_{dc}/2$

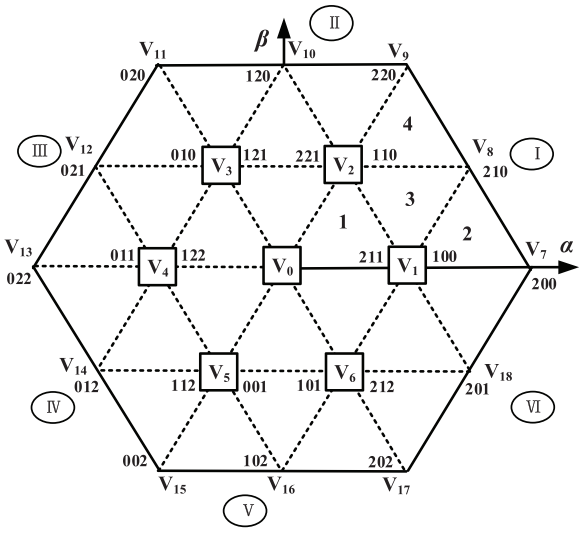

Fig. 2. Space vector diagram of three level NPC inverter.

voltages is defined by

$$V_{ref} = 2\left(V_a + V_b \cdot e^{j2\pi/3} + V_c \cdot e^{-j2\pi/3}\right)/3 . \quad (1)$$

By using Clark transformation, three-phase coordinate system *a*-*b*-*c* is transformed to 2-dimentional α-β frame which is helpful in sector identification by following expression:

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

where $V_{r\alpha}$ and $V_{r\beta}$ are the components of reference vector in α-β coordinate system. The reference voltage vector can be located in any region (1-4) of any sector (I-VI) in space vector diagram as shown in Fig. 2. For example, considering that the reference vector V_{ref} is locating in region 2 of sector I, the nearest three voltage vectors for this region are V_1, V_7 and V_8 are shown in Fig. 3.

After identification of nearest three vectors, the following expressions can be developed for the on-time calculations of the corresponding vectors by using the volt-second balance method

$$\left.\begin{aligned} V_{ref} T_s &= V_8 t_a + V_1 t_b + V_7 t_c \\ T_s &= t_a + t_b + t_c \end{aligned}\right\} \quad (3)$$

where T_s is the sampling time, t_a, t_b and t_c are the on-times for

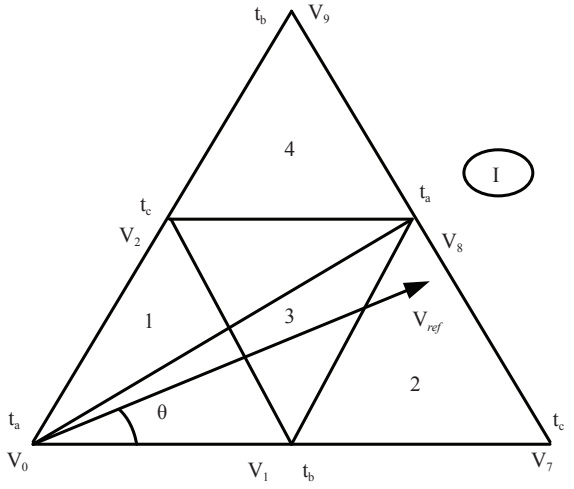

Fig. 3. Vector representation in sector I.

the voltage vectors V_8, V_1 and V_7 respectively. By solving (3), the on-time of the corresponding vectors can be computed by

$$\left.\begin{aligned} t_a &= a\sin\theta/\sqrt{3} \\ t_b &= 2T_s - a\sin\left(\theta+\pi/3\right)/\sqrt{3} \\ t_c &= -T_s - a\sin\left(\theta-\pi/3\right)/\sqrt{3} \end{aligned}\right\} \tag{4}$$

where a=3T_s (V_{ref}/ V_{dc}). The on-times for all the corresponding vectors in remaining regions of sector I can be computed by using similar procedure as expressed in TABLE II.

TABLE II
ON-TIMES IN SECTOR I

	t_a	t_b	t_c
Region 1	$T_s - a\sin(\theta + \pi/3)/\sqrt{3}$	$-a\sin(\theta - \pi/3)/\sqrt{3}$	$a\sin\theta/\sqrt{3}$
Region 2	$a\sin\theta/\sqrt{3}$	$2T_s - a\sin(\theta + \pi/3)/\sqrt{3}$	$-T_s - a\sin(\theta - \pi/3)/\sqrt{3}$
Region 3	$-T_s + a\sin(\theta + \pi/3)/\sqrt{3}$	$T_s - a\sin\theta/\sqrt{3}$	$T_s + a\sin(\theta - \pi/3)/\sqrt{3}$
Region 4	$-a\sin(\theta - \pi/3)/\sqrt{3}$	$-T_s + a\sin\theta/\sqrt{3}$	$2T_s - a\sin(\theta + \pi/3)/\sqrt{3}$

The next step in implementation of SVPWM is the selection of optimal switching sequence of the redundant states which is helpful in balancing of DC link capacitor voltages, fault tolerance and switching frequency reduction etc. TABLE III shows all possible switching sequence for all regions of sector I and Fig. 4 is the graphical representation for region 2.

The conventional SVPWM requires a huge amount of trigonometric operations to calculate the on-times of the switches which needs more storage space and additional hardware. There are three types of trigonometric functions (sinθ, sin(θ+π/3), sin(θ-π/3)) in TABLE I. These trigonometric functions can be converted into simplified line voltages form by using few calculations as follows:

TABLE III
POSSIBLE SWTTCHING SEQUENCE FOR SECTOR I

Region	Switching Sequence
1	(i) 222-221-211-111 (ii) 000-100-110-111 (iii) 221-211-111-110 (iv) 211-111-110-100
2	(i) 221-211-210-110 (ii) 211-210-110-100
3	221-220-210-110
4	211-210-200-100

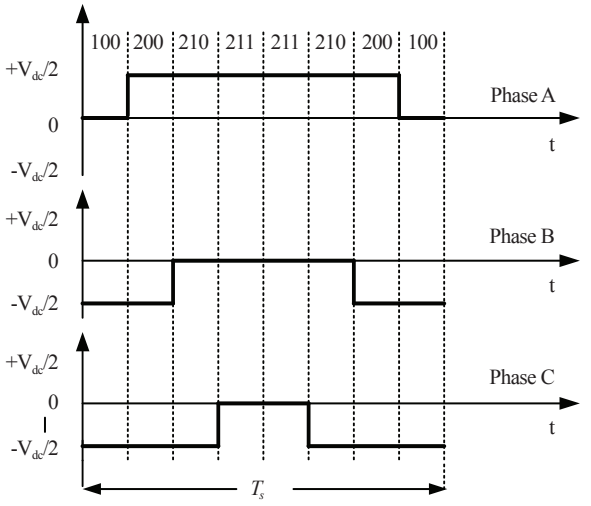

Fig. 4. Switching sequence for region 2.

$$|V_{ref}|\sin\theta = |V_{ref}|\sqrt{\tan^2\theta/(1+\tan^2\theta)} \tag{5}$$

$$|V_{ref}| = \sqrt{\frac{2}{3}\left[\left(V_a - \frac{1}{2}V_b - \frac{1}{2}V_c\right)^2 + \left(\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c\right)^2\right]} \tag{6}$$

$$\tan\theta = \frac{\mathrm{Re}(V_{ref})}{\mathrm{Im}(V_{ref})} = \frac{\frac{\sqrt{3}}{2}V_b - \frac{\sqrt{3}}{2}V_c}{V_a - \frac{1}{2}V_b - \frac{1}{2}V_c} \tag{7}$$

By using (6) and (7) into (5), the result in simplified line voltages form is

$$|V_{ref}|\sin\theta = V_{bc}/\sqrt{3} \tag{8}$$

The remaining two trigonometric functions can be calculated by using same method and the results are shown in (9) and (10).

$$|V_{ref}|\sin(\theta + \pi/3) = -V_{ca}/\sqrt{3} \tag{9}$$

$$|V_{ref}|\sin(\theta - \pi/3) = -V_{ab}/\sqrt{3} \tag{10}$$

Now the complex computations of the conventional SVPWM algorithm are converted into simplified line voltages form by replacing the values of trigonometric functions as shown in TABLE IV.

TABLE IV
ON-TIMES IN LINE VOLTAGES FORM FOR SECTOR I

	t_a	t_b	t_c
Region 1	$T_s\left(1+\frac{V_{ca}}{V_{dc}}\right)$	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\frac{V_{bc}}{V_{dc}}$
Region 2	$T_s\frac{V_{bc}}{V_{dc}}$	$T_s\left(2+\frac{V_{ca}}{V_{dc}}\right)$	$T_s\left(-1+\frac{V_{ab}}{V_{dc}}\right)$
Region 3	$T_s\left(-1-\frac{V_{ca}}{V_{dc}}\right)$	$T_s\left(1-\frac{V_{bc}}{V_{dc}}\right)$	$T_s\left(1-\frac{V_{ab}}{V_{dc}}\right)$
Region 4	$T_s\frac{V_{ab}}{V_{dc}}$	$T_s\left(-1+\frac{V_{bc}}{V_{dc}}\right)$	$T_s\left(2+\frac{V_{ca}}{V_{dc}}\right)$

III. SVPWM BASED ON *g-h* COORDINATE SYSTEM

The space vector diagram for three-level inverter based on 60° coordinate system is shown in Fig. 5. The *g*-axis overlapped with *α*-axis and the *h*-axis is 60° apart from *g*-axis in counter-clockwise direction.

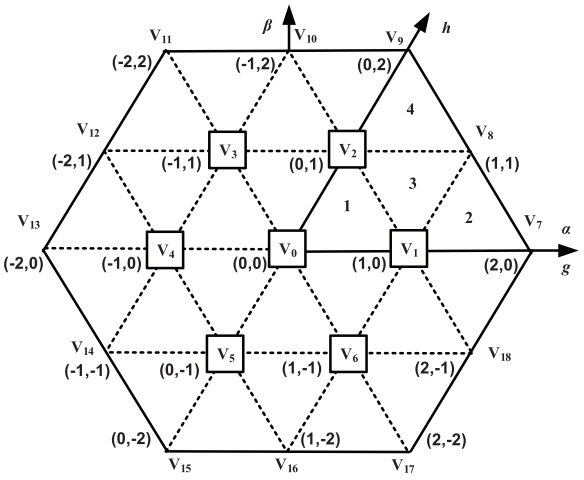

Fig. 5. Space vector diagram of inverter in g-h frame.

A. Coordinate Transformation

The transformation of reference vector V_{ref} from three-phase system to two dimensional *g-h* frame is the basic step of this algorithm. The relation between *α-β* coordinate system and *g-h* coordinate system is given by

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \begin{bmatrix} 1 & 1/2 \\ 0 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{rg} \\ V_{rh} \end{bmatrix} \tag{11}$$

and

$$\begin{bmatrix} V_{rg} \\ V_{rh} \end{bmatrix} = \begin{bmatrix} 1 & -1/\sqrt{3} \\ 0 & 2/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} \tag{12}$$

where V_{rg} and V_{rh} are the components of reference voltage vector V_{ref} in *g-h* coordinate system. By using (2) and (12) the desired coordinate transformation can be achieved as shown in the following expression.

$$\begin{bmatrix} V_{rg} \\ V_{rh} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{13}$$

Fig. 6 shows that the lines l_g, l_g+1, l_g+2..... are parallel to the *h*-axis and the projections of every vector located on these lines are gV_{dc}, (g+1) V_{dc}, (g+2) V_{dc}….. respectively on the *g*-axis. Similarly the lines l_h, l_h+1, l_h+2..... are parallel to the *g*-axis and the projections of every vector located on these lines are hV_{dc}, (h+1) V_{dc}, (h+2) V_{dc}….. respectively on the *h*-axis.

B. Identification of Nearest Three Vectors

All the switching vectors in *g-h* coordinate system have only integer coordinates, so the real values of the coordinates are rounded down to the integer values by using the *int*() function.

$$\left.\begin{aligned} g &= \text{int}(V_{rg}) \\ h &= \text{int}(V_{rh}) \end{aligned}\right\} \tag{14}$$

The nearest four vectors constitute a rhombus which is divided into triangle I and triangle II as shown in Fig. 6. The coordinates of vectors V_a, V_b, V_c and V_d are (*int* (V_{rg}), *int* (V_{rh})), (*int* (V_{rg})+1, *int* (V_{rh})), (*int* (V_{rg}), *int* (V_{rh})+1), and (*int* (V_{rg})+1, *int* (V_{rh})+1) respectively. The reference vector is locating in triangle I or triangle II, the decision can be made by the following expression:

$$\left.\begin{aligned} V_{ca}+1 \geq -(g+h) \quad & V_{ref} \text{ in triangle I} \\ V_{ca}+1 \leq -(g+h) \quad & V_{ref} \text{ in triangle II} \end{aligned}\right\} \tag{15}$$

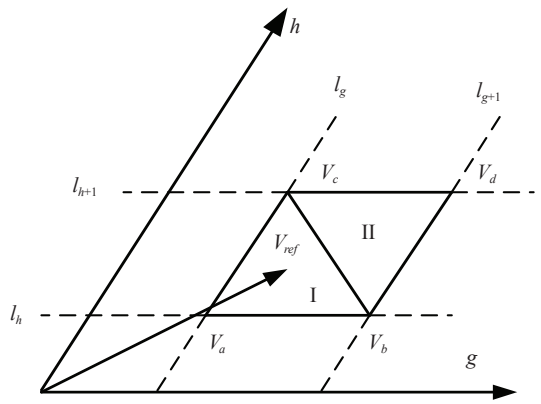

Fig. 6. The composition of space vector in g-h frame.

C. Duty Cycle Calculation

Assuming that the reference vector is locating in triangle I, the nearest three vectors are V_a, V_b and V_c. The duty ratio of the corresponding vectors can be calculated by

$$\left.\begin{aligned} V_{ref}T_s &= V_a t_a + V_b t_b + V_c t_c \\ T_s &= t_a + t_b + t_c \end{aligned}\right\}. \tag{16}$$

Transforming (16) into *g*-*h* coordinates yields

$$\left.\begin{aligned} V_{rg}T_s &= V_{ag}t_{g,h} + V_{bg}t_{g+1,h} + V_{cg}t_{g,h+1} \\ V_{rh}T_s &= V_{ah}t_{g,h} + V_{bh}t_{g+1,h} + V_{ch}t_{g,h+1} \\ T_s &= t_{g,h} + t_{g+1,h} + t_{g,h+1} \end{aligned}\right\}. \tag{17}$$

By solving (17), the on-time of the corresponding vectors can be computed by

$$\left.\begin{aligned} t_{g,h} &= T_s\left((V_{ca}/V_{dc}) + g + h + 1\right) \\ t_{g+1,h} &= T_s\left((V_{ab}/V_{dc}) - g\right) \\ t_{g,h+1} &= T_s\left((V_{bc}/V_{dc}) - h\right) \end{aligned}\right\}. \tag{18}$$

Similarly, when the reference vector is locating in triangle II, the on-times for the vectors V_b, V_c and V_d can be calculated by

$$\left.\begin{aligned} t_{g+1,h} &= T_s\left(-(V_{bc}/V_{dc}) + g + 1\right) \\ t_{g,h+1} &= T_s\left(-(V_{ab}/V_{dc}) + g + 1\right) \\ t_{g+1,h+1} &= T_s\left(-(V_{ca}/V_{dc}) - g - h - 1\right) \end{aligned}\right\}. \tag{19}$$

Assuming that, the amplitude of reference vector is $1.386V_{dc}$ and it is 25° electrical with respect to the *a*-axis. The corresponding line voltages are

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = 1.386 \cdot V_{dc} \begin{bmatrix} 0.574 \\ 0.422 \\ -0.966 \end{bmatrix} \tag{20}$$

and the value of V_{rg} and V_{rh} is $0.795V_{dc}$ and $0.585V_{dc}$ respectively. The exact location of reference vector can be determined by using (15).

$$V_{ca} + 1 \le -\left(g + h\right) = -0.380 < 0 \tag{21}$$

The reference vector is located in triangle 3 in Fig. 5 and the nearest three vectors are $V_1(1, 0)$, $V_2(0, 1)$ and $V_8(1, 1)$. The duty cycle for these vectors is calculated by (19).

$$\left.\begin{aligned} t_1 &= 0.415T_s \\ t_2 &= 0.205T_s \\ t_8 &= 0.380T_s \end{aligned}\right\} \tag{22}$$

D. Switching-State Selection

The last step of the algorithm is to transform the two-dimensional system back to three-dimensional switching states by using the following expression:

$$\begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} = \begin{bmatrix} i \\ i-g \\ i-h \end{bmatrix} \in (0,1,2), \quad i \in (0,1,2) \tag{23}$$

For example, the vectors (0, 1) and (1, 1) in the Fig. 5 can be transformed into (1 1 0), (2 2 1) and (2 1 0) switching states respectively.

IV. SVPWM Based on *K-L* Coordinate System

The *K-L* coordinate system is also called 120° coordinate system. Fig. 7 shows the space vector diagram for three-level inverter based on *K-L* coordinate system. The *L*-axis coincided with *α*-axis and the *K*-axis is 120° apart from *L*-axis in counter-clockwise direction.

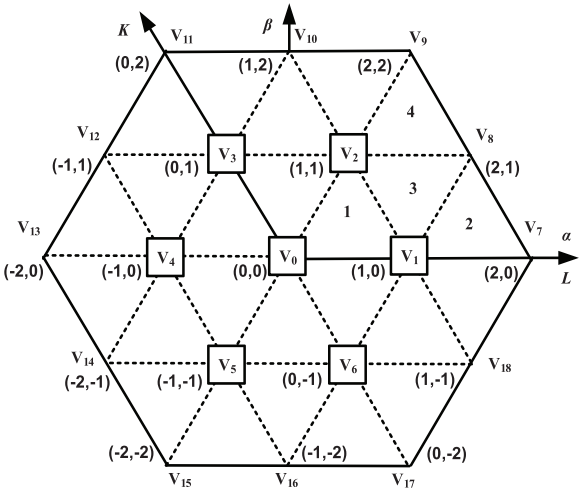

Fig. 7. Space vector diagram of inverter in K-L frame.

A. Coordinate Transformation

The initial step that is required in this algorithm is the transformation of reference vector V_{ref} from three-dimensional system to two dimensional *K-L* coordinate system. The relation between *α-β* coordinate system and *K-L* coordinate system is given by

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \begin{bmatrix} 1 & -1/2 \\ 0 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{rL} \\ V_{rK} \end{bmatrix} \tag{24}$$

and

$$\begin{bmatrix} V_{rL} \\ V_{rK} \end{bmatrix} = \begin{bmatrix} 1 & 1/\sqrt{3} \\ 0 & 2/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} \tag{25}$$

where V_{rL} and V_{rK} are the components of reference voltage vec-

tor V_{ref} in *K-L* coordinate system while $V_{r\alpha}$ and $V_{r\beta}$ are the components of V_{ref} in α-β coordinate system. By using (2) and (25) the desired coordinate transformation can be achieved as shown in the following expression:

$$\begin{bmatrix} V_{rL} \\ V_{rK} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}. \tag{26}$$

The lines l_L, l_L+1, l_L+2..... are parallel to the *K*-axis and the components of every vector located on these lines are LV_{dc}, (L+1) V_{dc}, (L+2) V_{dc}….. respectively on the *L*-axis as shown in Fig. 8. Similarly the lines l_K, l_K+1, l_K+2..... are parallel to the *L*-axis and the components of every vector located on these lines are KV_{dc}, (K+1) V_{dc}, (K+2) V_{dc}….. respectively on the *K*-axis.

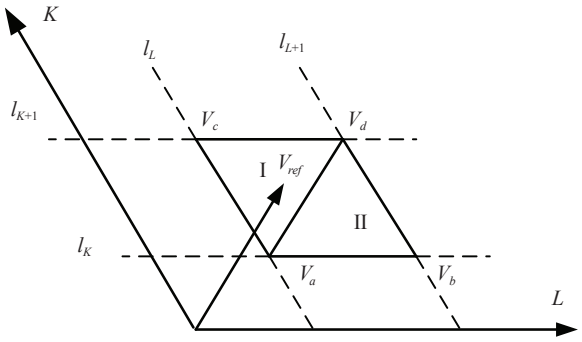

Fig. 8. The composition of space vector in K-L frame.

B. Identification of Nearest Three Vectors

As shown in Fig. 7, all the switching vectors in *K-L* coordinate system have only integer coordinates, so the real values of the coordinates are rounded down to the integer values by using the *int*() function.

$$\left.\begin{aligned} L &= \text{int}(V_{rL}) \\ K &= \text{int}(V_{rK}) \end{aligned}\right\} \tag{27}$$

The coordinates of the nearest four vectors V_a, V_b, V_c and V_d are (*int* (V_{rL}), *int* (V_{rK})), (*int* (V_{rL})+1, *int* (V_{rK})), (*int* (V_{rL}), *int* (V_{rK})+1) and (*int* (V_{rL})+1, *int* (V_{rK})+1) respectively. Whether the reference vector is locating in triangle I or triangle II, the decision can be made by the following expression:

$$\left.\begin{aligned} V_{ab} \le L-K \quad & V_{ref} \text{ in triangle I} \\ V_{ab} \ge L-K \quad & V_{ref} \text{ in triangle II} \end{aligned}\right\} \tag{28}$$

C. Duty Cycle Calculation

Assuming that the reference vector is locating in triangle I, the nearest three vectors are V_a, V_c and V_d. The duty ratio of the corresponding vectors can be calculated by

$$\left.\begin{aligned} V_{ref}T_s &= V_a t_a + V_c t_c + V_d t_d \\ T_s &= t_a + t_c + t_d \end{aligned}\right\}. \tag{29}$$

Transforming (29) into *K-L* coordinates yields

$$\left.\begin{aligned} V_{rL}T_s &= V_{aL}t_{L,K} + V_{cL}t_{L,K+1} + V_{dL}t_{L+1,K+1} \\ V_{rh}T_s &= V_{aK}t_{L,K} + V_{cK}t_{L,K+1} + V_{dK}t_{L+1,K+1} \\ T_s &= t_{L,K} + t_{L,K+1} + t_{L+1,K+1} \end{aligned}\right\}. \tag{30}$$

By solving (30), the on-time of the corresponding vectors can be computed by

$$\left.\begin{aligned} t_{L,K} &= T_s\left(-(V_{bc}/V_{dc}) + K + 1\right) \\ t_{L,K+1} &= T_s\left(-(V_{ab}/V_{dc}) + L - K\right) \\ t_{L+1,K+1} &= T_s\left(-(V_{ca}/V_{dc}) - L\right) \end{aligned}\right\}. \tag{31}$$

Similarly, when the reference vector is locating in triangle II, the on-times for the vectors V_a, V_b and V_d can be calculated by

$$\left.\begin{aligned} t_{L,K} &= T_s\left((V_{ca}/V_{dc}) + L + 1\right) \\ t_{L+1,K} &= T_s\left((V_{ab}/V_{dc}) - L + K\right) \\ t_{L+1,K+1} &= T_s\left((V_{bc}/V_{dc}) - K\right) \end{aligned}\right\}. \tag{32}$$

For example, by keeping the amplitude and angle of the reference vector same as *g-h* coordinate system, the value of V_{rL} and V_{rK} is $1.380V_{dc}$ and $0.585V_{dc}$ respectively. The exact location of reference vector can be determined by using (28).

$$V_{ab} \le L - K = 0.795 < 1 \tag{33}$$

The reference vector is located in triangle 3 in Fig. 7 and the nearest three vectors are V_1(1, 0), V_2(0, 1) and V_8(1, 1). The duty cycle for these vectors is calculated by (31).

$$\left.\begin{aligned} t_1 &= 0.415T_s \\ t_2 &= 0.205T_s \\ t_8 &= 0.380T_s \end{aligned}\right\} \tag{34}$$

D. Switching-State Selection

The last step of the algorithm is to transform the two-dimensional system back to three-dimensional switching states by using the following expression.

$$\begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} = \begin{bmatrix} i+L \\ i+K \\ i \end{bmatrix} \in (0,1,2), \quad i \in (0,1,2) \tag{35}$$

For example, the vectors (1, 0) and (2, 0) in the Fig. 7 can be transformed into (1 0 0), (2 1 1) and (2 0 0) switching states

respectively.

V. SVPWM Based on α′-β′ Coordinate System

The conventional SVPWM algorithm is based on α-β coordinate system and reference vector rotates in a circular trajectory. In this algorithm, circular trajectory of reference vector is transformed into an elliptical trajectory in α′-β′ frame as shown in Fig. 9.

A. Coordinate Transformation

The relationship between α-β frame and α′-β′ frame is given by

$$\begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} = \begin{bmatrix} 1/2 & -1/2 \\ \sqrt{3}/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} V_{r\alpha'} \\ V_{r\beta'} \end{bmatrix} \tag{36}$$

and

$$\begin{bmatrix} V_{r\alpha'} \\ V_{r\beta'} \end{bmatrix} = \begin{bmatrix} 1 & 1/\sqrt{3} \\ -1 & 1/\sqrt{3} \end{bmatrix} \begin{bmatrix} V_{r\alpha} \\ V_{r\beta} \end{bmatrix} \tag{37}$$

where $V_{r\alpha'}$ and $V_{r\beta'}$ are the components of reference voltage vector V_{ref} in α′-β′ coordinate system. The coordinate transformation from three-phase system to α′-β′ frame can be achieved by using (2) and (37) as shown in (38).

$$\begin{bmatrix} V_{r\alpha'} \\ V_{r\beta'} \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{38}$$

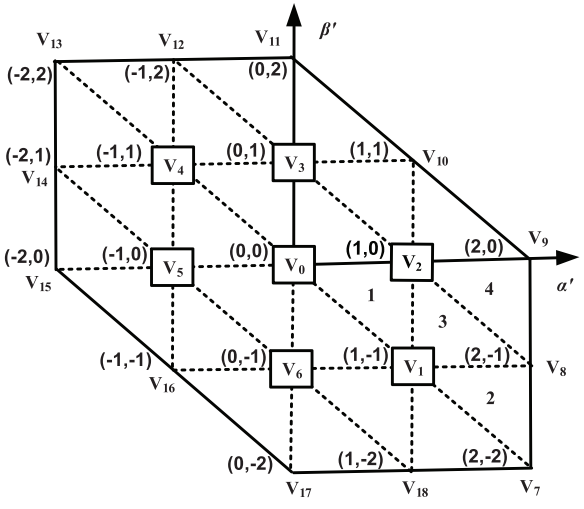

Fig. 9. Space vector diagram of inverter in α'-β' frame.

B. Identification of Nearest Three Vectors

As shown in Fig. 10, the vertices of the vectors V_a, V_b and V_c constitute triangles I and triangle II is made by the vertices of the vectors V_b, V_c and V_d. The coordinates of the nearest four vectors V_a, V_b, V_c and V_d are (*int* ($V_{r\alpha'}$), *int* ($V_{r\beta'}$)), (*int* ($V_{r\alpha'}$)+1, *int* ($V_{r\beta'}$)), (*int* ($V_{r\alpha'}$), *int* ($V_{r\beta'}$)+1) and (*int* ($V_{r\alpha'}$)+1, *int* ($V_{r\beta'}$)+1) respectively. *int*() is a function that is used to round down the real values to the integer values of the coordinates.

$$\left.\begin{aligned} \alpha' &= \mathrm{int}(V_{r\alpha'}) \\ \beta' &= \mathrm{int}(V_{r\beta'}) \end{aligned}\right\} \tag{39}$$

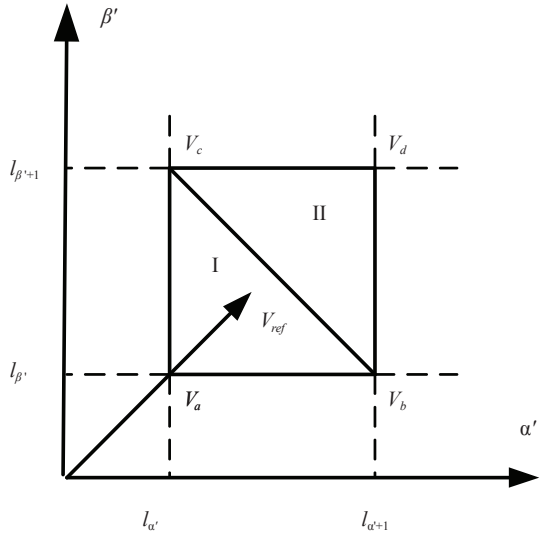

Fig. 10. The composition of space vector in α'-β' frame.

Vectors V_b and V_c are always the nearest two vectors while the third nearest vector will be decided by the following expression:

$$W = V_{bc} - \alpha' - \beta' - 1 . \tag{40}$$

If W<0, the third nearest vector will be V_a and V_{ref} will be located in triangle I; otherwise, reference vector will be in triangle II.

C. Duty Cycle Calculation

Assuming that the reference vector is locating in triangle I, the nearest three vectors are V_a, V_b and V_c. The duty ratio of the corresponding vectors can be calculated by

$$\left.\begin{aligned} V_{ref} T_s &= V_a t_a + V_b t_b + V_c t_c \\ T_s &= t_a + t_b + t_c \end{aligned}\right\} . \tag{41}$$

Transforming (41) into α′-β′ coordinates yields

$$\left.\begin{aligned} V_{r\alpha'} T_s &= V_{a\alpha'} t_{\alpha',\beta'} + V_{b\alpha'} t_{\alpha'+1,\beta'} + V_{c\alpha'} t_{\alpha',\beta'+1} \\ V_{r\beta'} T_s &= V_{a\beta'} t_{\alpha',\beta'} + V_{b\beta'} t_{\alpha'+1,\beta'} + V_{c\beta'} t_{\alpha',\beta'+1} \\ T_s &= t_{\alpha',\beta'} + t_{\alpha'+1,\beta'} + t_{\alpha',\beta'+1} \end{aligned}\right\} . \tag{42}$$

By solving (42), the on-time of the corresponding vectors can

be computed by

$$\left.\begin{aligned} t_{\alpha',\beta'} &= T_s\left(-(V_{bc}/V_{dc})+\alpha'+\beta'+1\right) \\ t_{\alpha'+1,\beta'} &= T_s\left(-(V_{ca}/V_{dc})-\alpha'\right) \\ t_{\alpha',\beta'+1} &= T_s\left(-(V_{ab}/V_{dc})-\beta'\right) \end{aligned}\right\}. \tag{43}$$

Similarly, when the reference vector is locating in triangle II, the on-times for the vectors V_b, V_c and V_d can be calculated by

$$\left.\begin{aligned} t_{\alpha'+1,\beta'} &= T_s\left((V_{ab}/V_{dc})+\beta'+1\right) \\ t_{\alpha',\beta'+1} &= T_s\left((V_{ca}/V_{dc})+\alpha'+1\right) \\ t_{\alpha'+1,\beta'+1} &= T_s\left((V_{bc}/V_{dc})-\alpha'-\beta'-1\right) \end{aligned}\right\}. \tag{44}$$

As an example, consider that the amplitude of reference vector is $1.386V_{dc}$ and the angle is 25° same as used in previous algorithms. So, the line voltages remain same and the value of $V_{r\alpha'}$ and $V_{r\beta'}$ is given by

$$\begin{bmatrix} V_{r\alpha'} \\ V_{r\beta'} \end{bmatrix} = V_{dc}\begin{bmatrix} 1.380 \\ -0.795 \end{bmatrix}. \tag{45}$$

The exact location of reference vector can be determined by the sign of (40).

$$W = V_{bc}-\alpha'-\beta'-1 = 0.585-1+1-1 = -0.415 \tag{46}$$

The sign of the above expression is negative so the reference vector is located in triangle 3 in Fig. 9 and the nearest three vectors are $V_1(1, -1)$, $V_2(1, 0)$ and $V_8(2, -1)$. The duty cycle for these vectors is calculated by (43).

$$\left.\begin{aligned} t_1 &= 0.415T_s \\ t_2 &= 0.205T_s \\ t_8 &= 0.380T_s \end{aligned}\right\} \tag{47}$$

D. Switching-State Selection

The last step of the algorithm is to transform the two-dimensional system back to three-dimensional switching states by using the following expression:

$$\begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} = \begin{bmatrix} i \\ i+\beta' \\ i-\alpha' \end{bmatrix} \in (0,1,2), \quad i \in (0,1,2). \tag{48}$$

For example, the vectors (0, -1) and (-1, 2) in the Fig. 9 can be transformed into (1 0 1), (2 1 2) and (0 2 1) switching states respectively.

VI. SVPWM Based on Imaginary Coordinate System

The space vector diagram for three-level inverter based on imaginary coordinate system is shown in Fig. 11. Three axis of imaginary coordinate system *ja*, *jb* and *jc* are perpendicular to the three-phase axis *a,b* and *c* respectively [52].

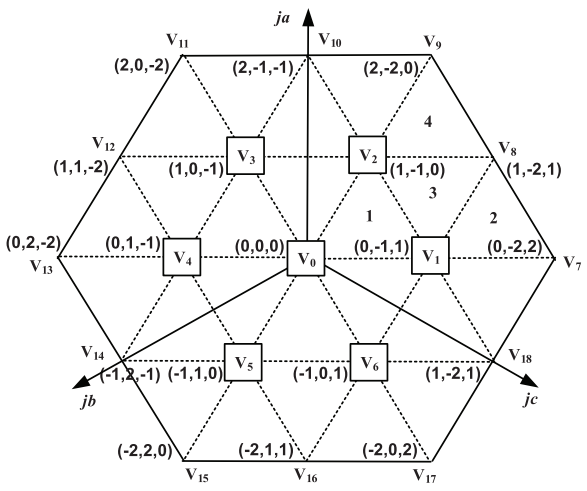

Fig. 11. Space vector diagram of inverter in *ja-jb-jc* frame.

A. Coordinate Transformation

The transformation from phase coordinate to the imaginary coordinate is given by

$$\begin{bmatrix} V_{ja} \\ V_{jb} \\ V_{jc} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{49}$$

where V_{ja}, V_{jb}, V_{jc} are variables of imaginary coordinate system and V_a, V_b, V_c are variables in phase coordinate system. The relation between imaginary frame and α-β frame is given by

$$\begin{bmatrix} V_{ja} \\ V_{jb} \\ V_{jc} \end{bmatrix} = \begin{bmatrix} 0 & \sqrt{2} \\ -\sqrt{3/2} & -1/\sqrt{2} \\ \sqrt{3/2} & -1/\sqrt{2} \end{bmatrix}\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix}. \tag{50}$$

B. Identification of Nearest Three Vectors

All the vectors in imaginary coordinate system have integer values as shown in Fig. 11. *int*() is a function that is used to rounded down the real values to the integer values: V_{ja}=*int* (V_{rja}), V_{jb}=*int* (V_{rjb}), V_{jc}=*int* (V_{rjc}). There are two possible directions of equilateral triangles as shown in Fig. 12. If *int* (V_{rja})+*int* (V_{rjb})+*int* (V_{rjc}) = -1, then the reference vector is locating in normal direction triangle and if *int* (V_{rja})+*int* (V_{rjb})+*int* (V_{rjc}) = -2, then the reference vector is locating in reverse direction triangle.

C. Duty Cycle Calculation

Assuming that the reference vector is locating in normal direction triangle. The coordinates of three vertices are (V_{ja}+1, V_{jb},

V_{jc}-1), (V_{ja}, V_{jb}+1, V_{jc}-1) and (V_{ja}, V_{jb}, V_{jc}). The time duration for these vertices is calculated by

$$\left.\begin{aligned} V_{ref} &= V_{ja}d_{ja} + V_{jb}d_{jb} + V_{jc}d_{jc} \\ d_{ja} + d_{jb} + d_{jc} &= 1 \end{aligned}\right\} \tag{51}$$

where $d_{ja}=h_a$, $d_{jb}=h_b$ and $d_{jc}=h_c$ are the duty ratio for the vertices and T_s is the sampling time. h_a, h_b and h_c represents the distance from the edges of triangle to the reference vector and computed by

$$\left.\begin{aligned} h_a &= V_{rja} - \mathrm{int}(V_{rja}) \\ h_b &= V_{rjb} - \mathrm{int}(V_{rjb}) \\ h_c &= V_{rjc} - \mathrm{int}(V_{rjc}) \end{aligned}\right\}. \tag{52}$$

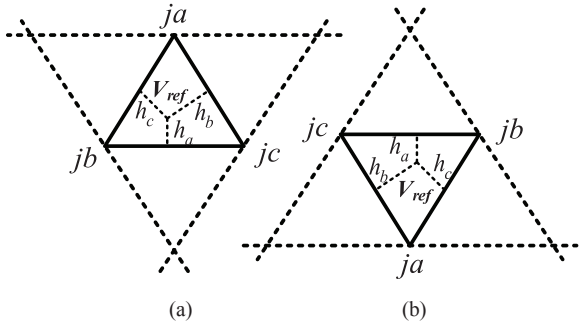

Fig. 12. Two possible directions of triangle. (a) normal direction and (b) reverse direction.

By using (51) and (52), the duty ratio for the corresponding vertices in line voltages form can be obtained by

$$\left.\begin{aligned} t_{ja} &= T_S\left((V_{bc}/V_{dc}) - V_{ja}\right) \\ t_{jb} &= T_S\left((V_{ca}/V_{dc}) - V_{jb}\right) \\ t_{jc} &= T_S\left((V_{ab}/V_{dc}) - V_{jc}\right) \end{aligned}\right\}. \tag{53}$$

Similarly, when the reference vector is locating in reverse direction triangle, the duty ratio for the corresponding vertices is calculated by

$$\left.\begin{aligned} t_{ja} &= T_S\left(-(V_{bc}/V_{dc}) + V_{ja} + 1\right) \\ t_{jb} &= T_S\left(-(V_{ca}/V_{dc}) + V_{jb} + 1\right) \\ t_{jc} &= T_S\left(-(V_{ab}/V_{dc}) + V_{jc} + 1\right) \end{aligned}\right\}. \tag{54}$$

For example, considering that the length and the angle of reference vector is $1.386V_{dc}$ and 25° respectively. The line voltages are given by

$$\begin{bmatrix} V_{ja} \\ V_{jb} \\ V_{jc} \end{bmatrix} = \begin{bmatrix} V_{bc} \\ V_{ca} \\ V_{ab} \end{bmatrix} = V_{dc}\begin{bmatrix} 0.585 \\ -1.380 \\ 0.795 \end{bmatrix}. \tag{55}$$

The exact location of reference vector, whether it is located in normal direction triangle or in reverse direction triangle is determined by the following expression:

$$\mathrm{int}(V_{rja}) + \mathrm{int}(V_{rjb}) + \mathrm{int}(V_{rjc}) = 0 - 2 + 0 = -2\,. \tag{56}$$

Because the value is -2, so the reference vector is located in reverse direction triangle and the nearest three vectors are V_1(0, -1, 1), V_2(1, -1, 0) and V_8(1, -2, 1). The duty cycle for these vectors is calculated by (54).

$$\left.\begin{aligned} t_{ja} &= t_1 = 0.415T_s \\ t_{jc} &= t_2 = 0.205T_s \\ t_{jb} &= t_8 = 0.380T_s \end{aligned}\right\} \tag{57}$$

D. Switching-State Selection

The last step of the algorithm is to transform the two-dimensional system back to three-dimensional switching states by using the following expression:

$$\begin{bmatrix} S_A \\ S_B \\ S_C \end{bmatrix} = \begin{bmatrix} i \\ i - jc \\ i + jb \end{bmatrix} \in (0,1,2), \quad i \in (0,1,2)\,. \tag{58}$$

For example, the vectors (1, -1, 0) and (0, -2, 2) in the Fig. 11 can be transformed into (2 2 1), (1 1 0) and (2 0 0) switching states respectively.

It is clear that the SVPWM based on imaginary coordinate is the simplest way in duty ratio calculations.

VII. Conclusion

This paper summarizes five different SVPWM algorithms for multilevel inverters which are *α-β* frame, *g-h* frame, *K-L* frame, *α′-β′* frame and SVPWM based on imaginary coordinate system. These algorithms are general and applicable to any level of inverter. Actually SVPWM is a modulation technique which is based on line voltage. Therefore, the complex computations of conventional SVPWM are converted into simplified line voltages form as shown in TABLE II and the duty cycles calculated for all other SVPWM algorithms are compared. As an example, for validation of the calculated results, the length and the angle of reference vector was kept constant for all the SVPWM algorithms and the on-time of the corresponding vectors is calculated. The comparison results validate all the SVPWM techniques, but the SVPWM based on imaginary coordinate is the simplest one in duty ratio calculations, easier to understand and provides a better control for zero-sequence component for any level of inverter.

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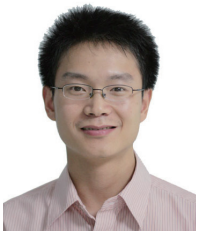

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Design of LCC Impedance Matching Circuit for Wireless Power Transfer System Under Rectifier Load

Chenglin Liao, Junfeng Li, and Shufan Li

***Abstract*—In wireless power transfer system, impedance matching circuits are usually used to match the impedance between actual load and the optimal load, to achieve the maximum transfer efficiency (coil to coil efficiency). It is easily to design impedance matching circuit parameters for linear load. However, the load is always the rectifier one in many applications. The equivalent impedance of rectifier load is complex impedance, which is affected not only by itself, but also by pre-stage circuit, such as impedance matching circuit parameters. It is hard to calculate the equivalent impedance of rectifier load directly to design the impedance matching circuit parameters. This paper investigates the LCC impedance matching design method for secondary side under rectifier load. Firstly, the transfer efficiency characteristic under rectifier load is studied, and the equivalent impedance is analyzed according to transfer efficiency. Then the impedance calculation method of secondary side under rectifier load is derived via formula derivation and Fourier series theory, and the LCC circuit parameters design method is proposed. Lastly, a wireless charging system for electric vehicle is established to verify the method that can transfer 3.3 kW power over 20 cm distance with 92.7% system efficiency (end to end efficiency).**

***Index Terms*—Impedance calculation, LCC Impedance matching, magnetic resonance coupling, optimization, rectifier load.**

I. Introduction

RECENTLY, wireless power transfer technology (WPT) is widely used in charging platforms of mobile device, biomedical implants, wireless sensor networks, electric vehicle, and many other applications [1]-[4].Compared to wired way, WPT is more safe, convenient, automated and environmentally adaptive. In 2007, a new WPT design method via magnetic resonant coupling (MRC) was proposed to enlarge the distance, improve the transmission power and efficiency, especially in middle range charging applications [5], [6].

For a common MRC system with two coils structure, primary coil and secondary coil, the circuit loop of secondary side is working at resonant condition [7], [8], and the transfer efficiency is affected by the coupling coefficient, quality factor, frequency, load and other parameters. There exists the optimum load value to achieve maximum transfer efficiency [9], [10]. However, the actual load is not always equal to the optimum value, so impedance matching circuits are used to match the impedance between actual load and optimum load [11]-[13]. There are many topologies of impedance matching circuit, and the circuit parameters can be easily designed using analytical or numerical method for linear load, such as resistive load, R-C (resistance and capacitance) load and R-L (resistance and inductance) load [14]-[17].

In many applications, such as electric vehicle wireless charger and mobile phone wireless charger, WPT system outputs are direct voltage and current, and always use rectifier circuit to convert high frequency alternating current into direct current, and then supply DC power for actual load, or other DC-DC converters [18]-[20]. Thus the load of secondary coil is a nonlinear rectifier load, and the impedance matching design becomes more complicated than linear load. The equivalent impedance of rectifier load is complex, containing resistive part and imaginary part, and the equivalent value is affected not only by its parameters, but also by the pre-stage impedance matching circuit, which cannot be easily simplified into linear impedance. So it is difficult to design the impedance matching circuit parameters for secondary side coil under rectifier load.

As mentioned in literature [21], a double-sided LCC compensation network and its tuning method was proposed for wireless EV charging system, which ensured the resonant frequency is irrelevant with the coupling coefficient between the two coils and is also independent of the load condition. But it doesn't take the nonlinear rectifier load into consideration. In literature [22], a Series/Series-Parallel topology was analyzed to achieve constant voltage output. In literature [23], the steady state track current was load independent using the LCL-T based impedance matching circuit. Despite various compensation methods, few of them were based on the nonlinear analysis of the rectifier load, instead considering the rectifier load as a resistance load.

This paper theoretically analyzes the working process of rectifier load together with LCC impedance matching circuit, and then deduces the analytical expressions of the voltage and current in circuit at each operation modes using Fourier series theory. Furthermore, the equivalent impedance calculation method of rectifier load is derived based on the fundamental component. Last but not the least, the secondary side impedance matching circuit parameters can be determined to achieve maximum transfer efficiency (coil to coil efficiency) for MRC system in an experimental way.

Manuscript received August 27, 2017. This work was supported by Beijing Municipal Science & Technology Commission under program under Grant D121100004512001.

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Digital Object Identifier 10.24295/CPSSTPEA.2017.00022

II. Basic Analysis of Wireless Power Transfer

A. Basic Theory Model Under Resistive Load

The simplified typical circuit of WPT system with two coils structure, as Fig. 1 shows, contains voltage source U_1, primary capacitor C_P, primary coil inductor L_P, primary coil resistor R_P, secondary capacitor C_S, secondary coil inductor L_S, secondary resistor R_S, and load R_L.M_{PS} is the mutual inductance between primary coil and secondary coil.

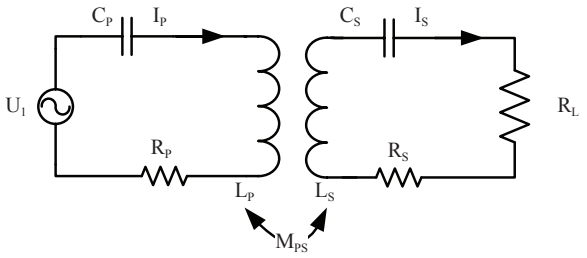


Fig. 1. Simplified typical circuit of WPT under resistance load.

The typical circuit can be described in matrix equations (1) [24]. The power loss P_t, load power P_L, and efficiency η satisfy (2)-(4), where ω is operation radian frequency.

$$\begin{bmatrix} U_1 \\ 0 \end{bmatrix} = \begin{bmatrix} j\omega L_P + 1/(j\omega C_P) + R_P & j\omega M_{PS} \\ j\omega M_{PS} & j\omega L_S + 1/(j\omega C_S) + R_S + R_L \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \quad (1)$$

$$P_t = I_P^2 R_P + I_S^2 R_S \quad (2)$$

$$P_L = I_S^2 R_L \quad (3)$$

$$\eta = 1/(1 + P_t / P_L) \quad (4)$$

Where I_P and I_S are the virtual values of the currents of primary and secondary side, respectively.

We use $y = P_t/P_L$, and calculate y in (5), where κ_{PS} is the coupling factor between coils, Q_P and Q_S is quality factor of primary and secondary coil, $Q_{P,S} = \omega L_{P,S}/R_{P,S}$.

$$y = \frac{\left| j\omega L_S + 1/(j\omega C_S) + R_S + R_L \right|^2}{\omega \kappa_{PS}^2 L_S Q_P R_L} + \frac{\omega L_S}{Q_S R_L} \quad (5)$$

So it is obviously that $\eta \propto Q_P$, Q_S, κ_{PS}, and reaches local maximum point at $j\omega L_s + 1/(j\omega C_s) = 0$.

Equation (5) can be simplified into (6) when parameters satisfy $j\omega L_s + 1/(j\omega C_s) = 0$.

$$y = \frac{(R_S + R_L)^2}{\omega \kappa_{PS}^2 L_S Q_P R_L} + \frac{\omega L_S}{Q_S R_L} \quad (6)$$

We can get the maximum efficiency η when y reaches its minimum point. The maximum condition in (7) is satisfied when R_L equals to the optimum value R_{opt}: $R_{opt} = R_S \sqrt{1 + k_{PS}^2 Q_P Q_S}$.

$$\frac{\partial y}{\partial R_L} = \frac{1}{w k_{PS}^2 L_S Q_P} - \frac{R_S^2}{w k_{PS}^2 L_S Q_P R_L^2} - \frac{w L_S}{Q_S R_L^2} = 0 \quad (7)$$

And then the maximum efficiency η_{max} can be calculated in (8)[25],

$$\eta_{max} = \Delta / (\sqrt{1+\Delta} + 1)^2 \quad (8)$$

$$\Delta = k_{PS}^2 Q_P Q_S \quad (9)$$

Therefore, if L_P, L_S, κ_{PS}, R_P, R_S are known, we can obtain the maximum efficiency conditions:

$$\begin{cases} C_S = 1/(\omega^2 L_S) \\ R_L = R_{opt} \end{cases} \quad (10)$$

B. Efficiency Characteristics Under Rectifier Load

In many applications, there is not always the resistive load of secondary side coil, but the rectifier load that contains rectifier diode, large capacitance C_L and resistance R_L, as Fig. 2 shows. The resistance R_L is the actual load for users, but the rectifier load is the real load for secondary side coil.

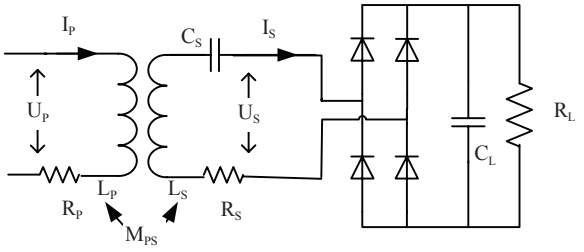


Fig. 2. Typical circuit of WPT system under rectifier load.

To study the effect of the rectifier load on the performance of the WPT system, a simulation is conducted in Matlab/Simulink test bench. The efficiency characteristic of WPT system under rectifier load is the same with system under resistance load, as Fig. 3 shows. There also exists the maximum efficiency point

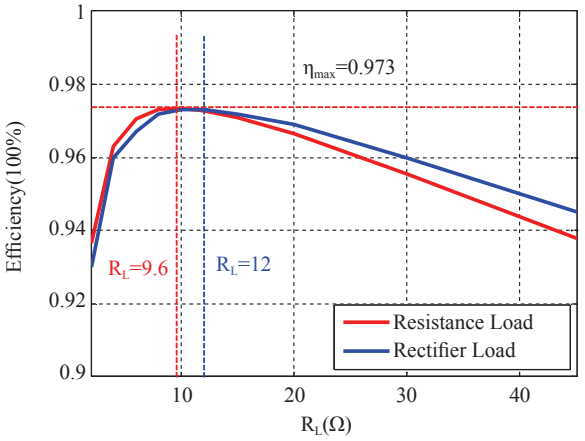


Fig. 3. Efficiency comparison between resistance load and rectifier load, where C_S= 61.1nF, C_S and L_S are working at resonant condition.

and the similar tendency, where parameters as TABLE I show.

TABLE I
WPT SYSTEM PARAMETER

Parameter	Value	Parameter	Value
L_P	164.26 *uH*	L_S	165.69 *uH*
R_P	0.101 *Ω*	R_S	0.129 *Ω*
M_{PS}	27.04 *uH*	*Frequency*	50 kHz
C_L	470 uF		

However, there are different efficiency characteristics between the two load types apparently. Firstly, the optimum R_L for maximum efficiency is different, as Fig. 3 shows, and larger in system under rectifier load. Secondly, at different R_L conditions, as Fig. 4 shows, the optimum capacitance C_S for WPT system under rectifier load is varying, while it is constant in system under resistance load that equals to $1/(\omega^2 L_S)$. According to Fig. 3 and Fig. 4, it can be indicated that the equivalent impedance of rectifier load is complex impedance, which contains real part and imaginary part, and the equivalent value is not only affected by its parameters, but also the pre-stage circuit parameter. When designing the impedance matching circuit between rectifier load and secondary coil, the characteristics must be taken into consideration.

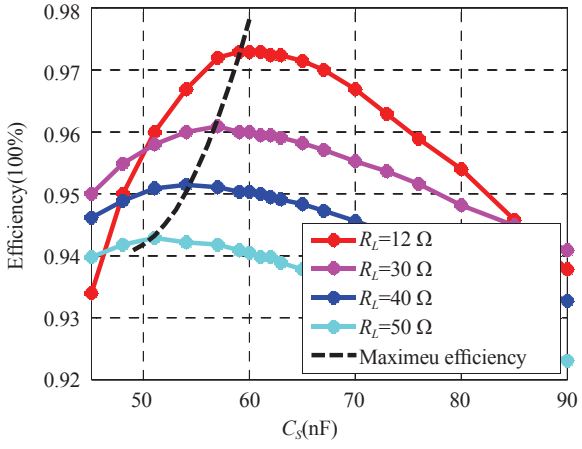


Fig. 4. Effects of C_S on efficiency at different R_L conditions of rectifier load.

III. Theory Analysis of Proposed Impedance Calculation Method for Rectifier Load Using LCC Impedance Matching Circuit

As is shown in section II, and optimum load R_{opt} should be obtained to achieve the maximum efficiency of the WPT system. However, it is obvious from Fig. 1 that the S-S impedance matching method cannot adjust the real part of the secondary side impedance, thus it cannot match the load to R_{opt} unless the real part of the rectifier load equals to R_{opt}. Taking the above analysis into consideration, the LCC impedance matching method is introduced to meet the optimum load R_{opt} for secondary coil for maximum efficiency in WPT system under rectifier load, as Fig. 5 shows, C_S, C_{21} and L_{21} forms LCC impedance matching circuit.

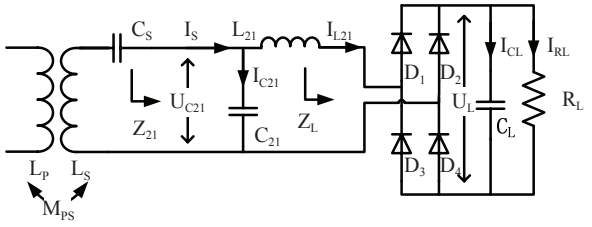


Fig. 5. LCC impedance matching circuit for rectifier load.

For conventional LCC impedance matching method, the rectifier load is seen as a resistance load. A simulation was conducted based on the data shown in TABLE I. Using the conventional LCC impedance matching method, rectifier load and resistance load were matched to the optimum load respectively, as Fig. 6 shows. It can be seen that with the conventional method, a relatively high efficiency can be achieved for resistance load, while for rectifier load, the efficiency is lower except for very small R_L. The main reason for this is that the rectifier load is seen as a resistance load in the conventional method, introducing errors which cannot be neglected. In the following part of this section, the rectifier load will be calculated to solve this problem.

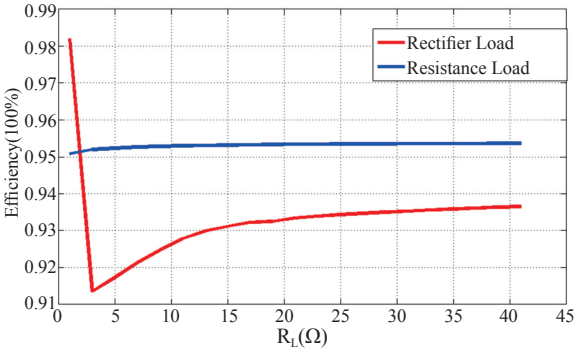


Fig. 6. Efficiency comparison between resistance load and rectifier load for conventional LCC impedance matching method.

A. Circuit Operation Analysis

Due to heavily affected by pre-stage circuit, rectifier load is combined with LCC circuit for impedance calculation. The equivalent impedance Z_{21} in Fig. 5 is analyzed to match R_{opt} via adjusting C_S, C_{21} and L_{21}.

Simulations have been conducted to study the circuit operation of the secondary side for LCC compensation method.Fig. 7 shows the operation current and voltage waveforms of secondary side circuit, of which the rectifier works in continuous conduction mode (CCM) (the working condition of the rectifier will be illustrated later). Though affected by diode nonlinear characteristic, the secondary coil current $i_S(t)$ is approximately sinusoidal waveform using LCC impedance matching circuit. We can regard i_S as a sinusoidal current source, $i_S(t)=I_S \sin(\omega t+\delta)$.

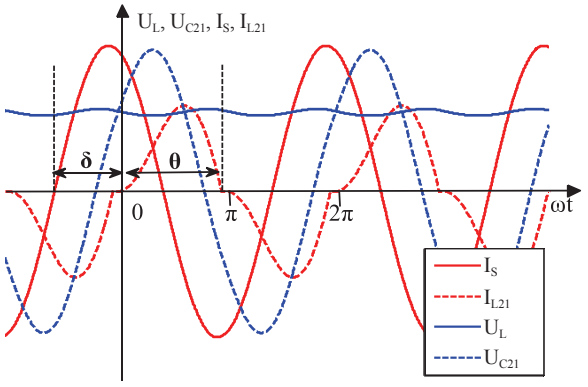


Fig. 7. Operation waveforms of LCC and Rectifier circuit (CCM state). δ is the rectifier diodes conduction lag, θ is the conduction angle of rectifier circuit.

The rectifier operation process can be described by four modes as Fig. 8 shows.

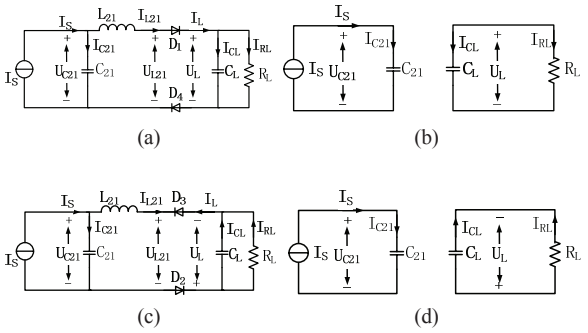


Fig. 8. Operation modes of rectifier load. (a) $0 \le \omega t < \theta$; (b) $\theta \le \omega t < \pi$; (c) $\pi \le \omega t < \pi + \theta$; (d) $\pi + \theta \le \omega t < 2\pi$.

(a) When $0 \le \omega t < \theta$:

We can establish the circuit equations as (11)-(14) according to Fig. 8(a). So $u_L(t)$ can be deduced in (15) .

$$i_{C21}(t) = C_{21}\frac{du_{C21}(t)}{dt} \tag{11}$$

$$i_{L21}(t) = \frac{u_L(t)}{R_L} + C_L\frac{du_L(t)}{dt} \tag{12}$$

$$i_{C21}(t) + i_{L21}(t) = I_S\sin(\omega t + \delta) \tag{13}$$

$$u_{C21}(t) = L_{21}\frac{di_{L21}(t)}{dt} + u_L(t) \tag{14}$$

$$\frac{d^3u_L(t)}{dt^3} + A\frac{d^2u_L(t)}{dt^2} + B\frac{du_L(t)}{dt} + Cu_L(t) = D\sin(\omega t + \delta) \tag{15}$$

Where $A = 1/(C_LR_L)$, $B = 1/(L_{21}C_{21}) + 1/(L_{21}C_L)$, $C = 1/(L_{21}C_{21}C_LR_L)$, $D = I_S/(L_{21}C_{21}C_L)$

We can obtain the characteristic equation as (16), and solve the roots $\lambda_1, \lambda_2, \lambda_3$ in (17)-(18).

$$\lambda^3 + A\lambda^2 + B\lambda + C = 0 \tag{16}$$

$$\lambda_1 = -(\frac{B}{3} - \frac{A^2}{9}) / \sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}}$$
$$- \frac{A}{3} + \sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}} \tag{17}$$

$$\lambda_{2,3} = (\frac{B}{3} - \frac{A^2}{9}) / \left[2 * \sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}}\right]$$
$$- \frac{A}{3} - \frac{1}{2}\sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}}$$
$$\pm i\frac{\sqrt{3}}{2}\left[(\frac{B}{3} - \frac{A^2}{9}) / \sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}}\right.$$
$$\left. + \sqrt[3]{\sqrt{(\frac{A^3}{27} - \frac{AB}{6} + \frac{C}{2})^2 + (\frac{B}{3} - \frac{A^2}{9})^3} - \frac{A^3}{27} + \frac{AB}{6} - \frac{C}{2}}\right] \tag{18}$$

It is obvious that λ_2, λ_3 can be described as $\lambda_{2,3} = \alpha \pm i\beta$. So the solution for homogenous equation of (15) can be described as (19), where C_1, C_2, C_3 are coefficients.

$$u_L(t) = C_1e^{\lambda_1} + e^{\alpha t}\left[C_2\cos(\beta t) + C_3\sin(\beta t)\right] \tag{19}$$

Based on further analysis, we can know that $\alpha < 0$, and $i\omega$ is not the solution of homogenous form of (15). The particular solution of (15) can be described in (20).The coefficient C_4 and C_5 are calculated by (21). Then $u_L(t)$, $i_{L2l}(t)$, $u_{C2l}(t)$ can be described in (22)-(24) when $0 \le \omega t < \theta$.

$$u_L^*(t) = C_4\cos(\omega t + \delta) + C_5\sin(\omega t + \delta) \tag{20}$$

$$\begin{bmatrix} \omega^3 - B\omega & C - A\omega^2 \\ C - A\omega^2 & -\omega^3 + B\omega \end{bmatrix}\begin{bmatrix} C_4 \\ C_5 \end{bmatrix} = \begin{bmatrix} D \\ 0 \end{bmatrix} \tag{21}$$

$$\begin{aligned} u_L(t) &= u_L(t) + u_L^*(t) \\ &= C_1e^{\lambda_1 t} + e^{\alpha t}\left[C_2\cos(\beta t) + C_3\sin(\beta t)\right] \\ &\quad + C_4\cos(\omega t + \delta) + C_5\sin(\omega t + \delta) \end{aligned} \tag{22}$$

$$\begin{aligned} i_{L21}(t) &= e^{\alpha t}(C_LC_3\beta + C_L\alpha C_2 + C_2/R_L)\cos(\beta t) \\ &\quad + e^{\alpha t}(C_L\alpha C_3 - C_LC_2\beta + C_3/R_L)\sin(\beta t) \\ &\quad + (C_LC_5\omega + C_4/R_L)\cos(\omega t + \delta) \\ &\quad + (C_5/R_L - C_LC_4\omega)\sin(\omega t + \delta) \\ &\quad + C_1e^{\lambda_1 t}(C_L\lambda_1 + 1/R_L) \end{aligned} \tag{23}$$

$$\begin{aligned} u_{C21}(t) &= [(\alpha^2 - \beta^2)C_LC_2 + 2\alpha\beta C_LC_3 + \frac{\alpha C_2 + \beta C_3}{R_L}]e^{\alpha t}\cos(\beta t) \\ &\quad + [(\alpha^2 - \beta^2)C_LC_3 - 2\alpha\beta C_LC_2 + \frac{\alpha C_3 - \beta C_2}{R_L}]e^{\alpha t}\sin(\beta t) \\ &\quad - \omega(C_LC_5\omega + C_4/R_L)\sin(\omega t + \delta) \\ &\quad + \omega(C_5/R_L - C_LC_4\omega)\cos(\omega t + \delta) \\ &\quad + C_1\lambda_1e^{\lambda_1 t}(C_L\lambda_1 + 1/R_L) \end{aligned} \tag{24}$$

β in (23) reflects the high frequency component in i_{L2l}(t), and

satisfies (25). It is obvious that the high frequency component of diodes current is closely related to L_{21}, and the frequency β can be very high when L_{21} is very low.

$$\beta \approx \sqrt{\frac{1}{L_{21}C_{21}}+\frac{1}{L_{21}C_L}-\frac{1}{3}\left(\frac{1}{C_L R_L}\right)^2} \approx \frac{1}{\sqrt{L_{21}C_{21}}} \tag{25}$$

(b) When $\theta \le \omega t < \pi$:

At that moment, rectifier diodes turn off, and $u_L(t)$, $u_{C21}(t)$ can be described in (26)-(27).

$$u_L(t) = u_L(\theta/\omega)e^{(\theta-t)/(\omega R_L C_L)} \tag{26}$$

$$u_{C21}(t) = \frac{1}{C_{21}}\int_{\theta/\omega}^{t} i_S(t)dt + u_{C21}\left(\frac{\theta}{\omega}\right) \tag{27}$$

(c) When $\pi \le \omega t < \pi + \theta$:

According to the cycle property, we can substitute $t-\pi/\omega$ for t in (24) to get the expression of $-u_{C2l}(t)$ when $\pi \le \omega t < \pi+\theta$.

(d) When $\pi+\theta \le \omega t < 2\pi$:

We can also substitute $t-\pi/\omega$ for t in (27) to get the expression of $-u_{C2l}(t)$ when $\pi+\theta \le \omega t < 2\pi$.

B. Calculation of Equivalent Impedance Z_{21}

According to circuit theory, expressions of $u_L(t)$, $i_{L2l}(t)$, $u_{C2l}(t)$ should satisfy initial conditions in (28)-(32), so we can solve C_1, C_2, C_3, δ.

$$i_{L21}(0) = 0 \tag{28}$$

$$i_{L21}\left(\frac{\theta}{\omega}\right)=0 \tag{29}$$

$$u_L(0) = u_L\left(\frac{\pi}{\omega}\right) \tag{30}$$

$$u_{C21}(0) = u_L(0) \tag{31}$$

$$u_{C21}\left(\frac{\pi}{\omega}\right) = -u_L\left(\frac{\pi}{\omega}\right) \tag{32}$$

Therefore, the expressions of $u_L(t)$, $i_{L2l}(t)$, $u_{C2l}(t)$ is determined. We use Fourier series theory to deduce the expression of $u_{C2l}(t)$ in whole cycle in (33).

$$u_{C21}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left[\sqrt{a_n^2+b_n^2}\sin(n\omega t+\varphi_n)\right] \text{(n=1,2...)} \tag{33}$$

$$a_n = \frac{\omega}{\pi}\int_{-\pi/\omega}^{\pi/\omega} u_{C21}(t)\cos(nt)dt \tag{34}$$

$$b_n = \frac{\omega}{\pi}\int_{-\pi/\omega}^{\pi/\omega} u_{C21}(t)\sin(nt)dt \tag{35}$$

$$\varphi_n = \arccos\frac{b_n}{\sqrt{a_n^2+b_n^2}} \tag{36}$$

In WPT system with optimal LCC impedance matching circuit, $u_{C2l}(t)$ is approximately like sinusoidal waveforms, and containing few harmonic distortion. We can use fundamental component to calculate the equivalent impedance of Z_{21} in Fig. 5 by (37).

$$Z_{21} = \frac{U_{C21}}{I_S} = \frac{\sqrt{a_1^2+b_1^2}}{I_S}e^{j(\varphi_1-\delta)} \tag{37}$$

$Z_{21} = R_{21} + jX_{21}$, where R_{21} and X_{21} are the real and imaginary part of Z_{21} respectively.

Then the equivalent impedance of rectifier load Z_L is computed in (38)

$$Z_L = \frac{Z_{21}}{1-i\omega C_{21}Z_{21}} - i\omega L_{21} \tag{38}$$

C. Special Operation Mode of LCC

When θ increases to π, the four rectifier operation modes translate into two modes as Fig. 9 shows. And we can also deduce the expression of $u_{C21}(t)$ and Z_{21} using the same method.

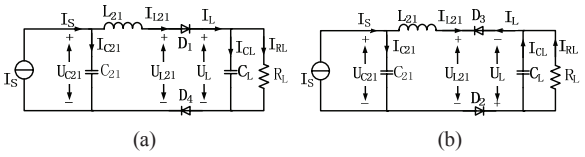


Fig. 9. Operation modes of rectifier load when $\theta = \pi$. (a) $0 \le \omega t < \pi$; (b) $\pi \le \omega t < 2\pi$.

D. Analysis of Rectifier Load Equivalent Impedance Z_R

Equivalent impedance Z_L of rectifier load can be calculated based on former analysis. The value of Z_L contains real part Z_{LR} and imaginary part X_{LR}, as Fig. 10-Fig. 11 shows. LCC circuit parameters C_{21} and L_{21} heavily affect Z_L value.

According to the results, both real and imaginary part of Z_L is not constant, which is causing problems on designing parameters for impedance matching circuit. As for linear load, we can design impedance matching circuit independently, because the load impedance and target impedance are definite. However, the equivalent impedance of rectifier load is time-varying, so a novel method to design the impedance matching parameters is in evitable to be put forward.

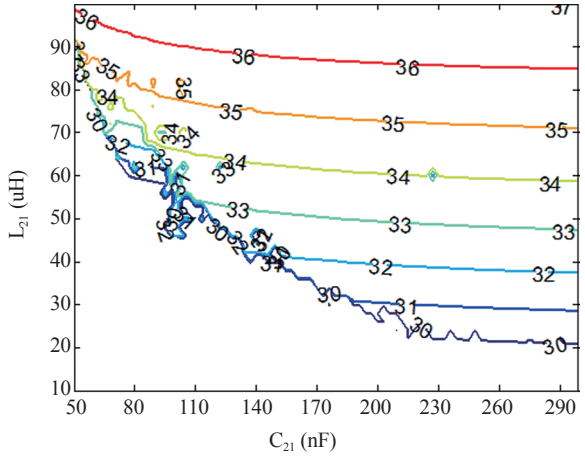


Fig. 10. The impedance impacts of L_{21} and C_{21} on R_{LR}, when R_L= 50 Ω.

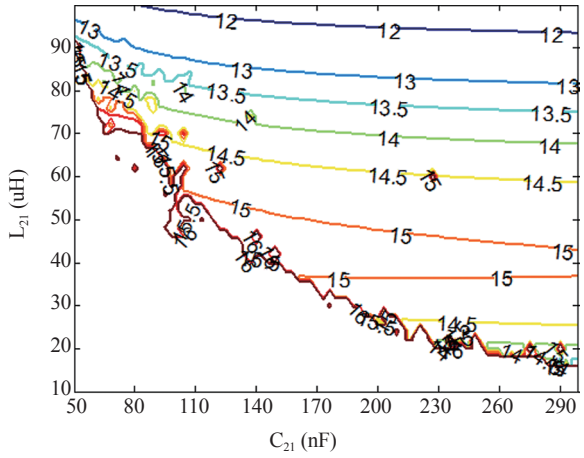


Fig. 11. The impedance impacts of L_{21} and C_{21} on X_{LR}, when R_L= 50 Ω.

Rectifier load only contains diodes, C_L and R_L, without inductance, but it is interesting that the equivalent impedance model of rectifier load can present *R-L* load.

IV. Design of LCC Parameters Under Rectifier Load

In order to meet the maximum efficiency condition, R_{21} is designed to equal R_{opt} by adjusting C_{21} and L_{21}, and secondary side circuit is tuned to resonant by C_S. According to the theory analysis, C_S is not necessary in some cases, and the impedance matching circuit can be translated into LCL topology.

When designing the LCC parameters L_{21}, C_{21} and C_S, there are many combinations satisfying the maximum efficiency condition. In order to choose one combination for WPT system, L_{21} or C_{21} can be determined firstly, and then compute others. According to the effect of L_{21} and C_{21} on R_{21}, as Fig. 12 shows, the value of C_{21} is more flexible to regulate R_{21}.

The variable β in (23) reflects the harmonic current in rectifier diodes, as Fig. 13 shows, which is even determined by L_{21} and C_{21}. When β becomes larger, the loss of diodes is obviously increasing because of the rectifier works from continuous

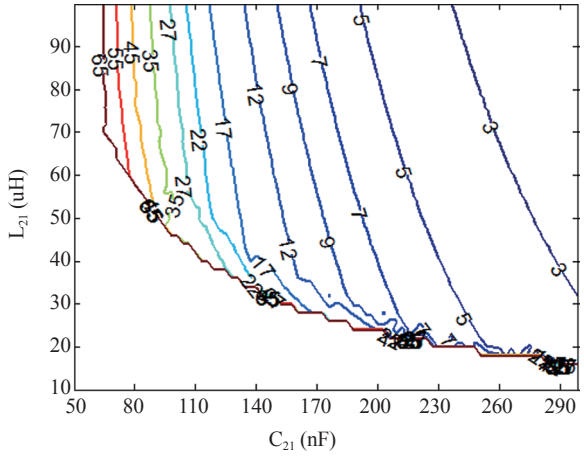


Fig. 12. The impedance impacts of L_{21} and C_{21} on R_{21}, when R_L= 50 Ω.

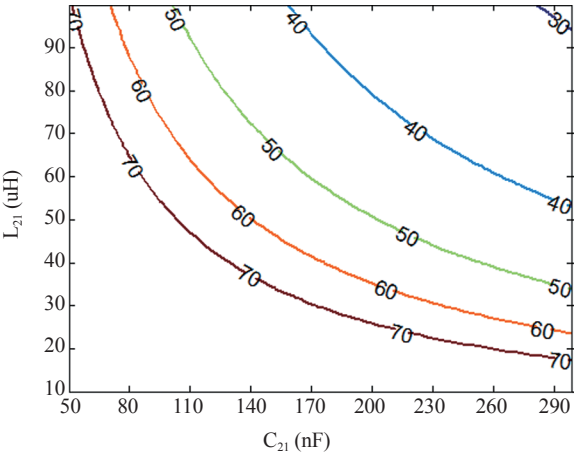
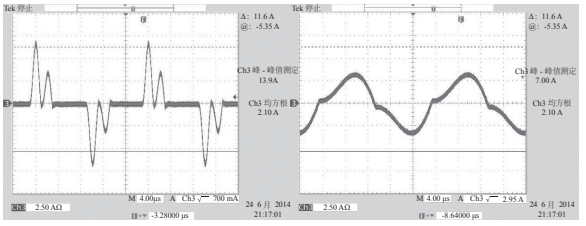


Fig. 13. The frequency impacts of L_{21} and C_{21} on high-frequency β (kHz), when R_L= 50 Ω.

conduction mode (CCM) to discontinuous conduction mode (DCM), meanwhile the peak current becomes larger, as Fig. 14 shows.



(a) Rectifier works in DCM (b) Rectifier works in CCM

Fig. 14. The current wave of rectifier diode using LCC impedance matching circuit. L_S= 165.7 uH, C_S= 117.3 nF, C_{21}= 161.9 nF, f=50 kHz.

It is obvious that we can increase L_{21} or C_{21} to decrease β value, and L_{21} is more suitable to enlarge the scope of impedance matching for rectifier load. Therefore, we can determine L_{21} firstly, and then compute C_{21} and C_S. L_{21} should be large enough to be optimized according to actual need, therefore, the initial value of L_{21} should be its maximum value, which can be determined according to experiences. When L_{21} is determined, we can analyze the effects of C_{21} on R_{21}, and decide its value according to $R_{21} = R_{opt}$. Then C_S can be tuned to resonant for secondary side circuit loop. If the conditions "$R_{21} = R_{opt}$" or "$Z_{21} = R_{opt}$" cannot be satisfied with the preset value of L_{21}, then its value should be decreased by 0.1μH in a loop until the conditions above are satisfied. A complete designing process of the secondary side LCC parameters is showed in Fig. 15.

After determining the value of the secondary side LCC network, the value of the primary side LCC network can be designed according to the conventional LCC compensation method [21]. It should be noticed that the value of "L", namely the inductance in the LCC network of the primary side, should be slightly larger(usually 10%~20%) than its theoretical value to guarantee an inductive load of the inverter, thus satisfying the ZVS condition of the system.

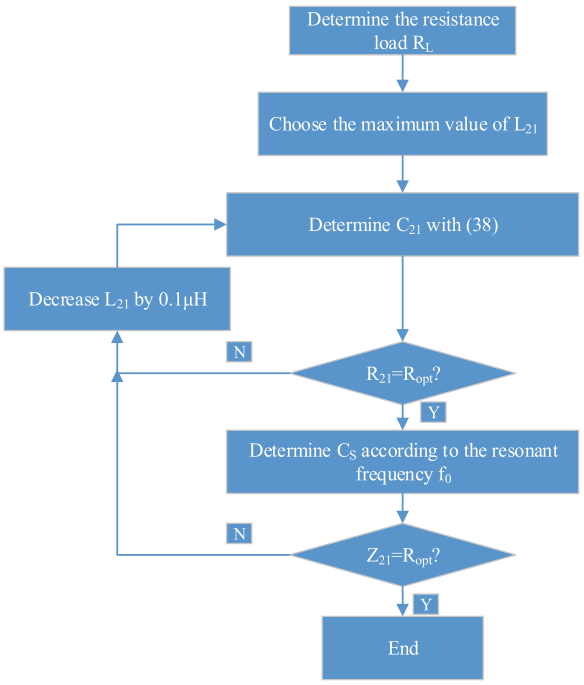


Fig. 15. Flowchart of the designing process of the LCC parameters.

V. Experimental Verification

Experiments are conducted to verify the design method of LCC impedance matching circuit under rectifier load. The WPT system is established as Fig. 16 shows, containing DC voltage source, voltage source inverter, primary coil and secondary coil, and dual-side LCC impedance matching circuits, rectifier circuit and load. The system parameters are shown in TABLE I.

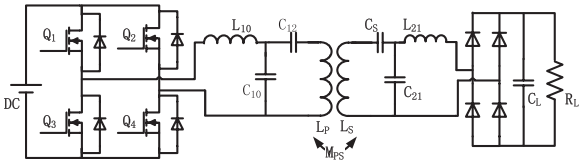


Fig. 16. WPT system circuit.

A. Impedance Matching for Different RL

According to WPT parameters in TABLE I, the optimal load for secondary coil and maximum efficiency can be theoretically calculated: R_{opt} = 9.6 Ω, and η_{max}= 97.35%. According to the proposed LCC impedance matching method, the rectifier load with different R_L can be matched by parameters in Fig. 17, where L_{21} = 86.1 uH. The transfer efficiency after LCC impedance matching is improved as Fig. 18 shows.

The transfer efficiency of the WPT system with the conventional C impedance matching(as Fig. 2 shows), the conventional LCC impedance matching [21] and the proposed LCC impedance matching is simulated separately. Due to the power losses of the converters and other components in the circuit, the efficiency does not reach the theoretical maximum efficiency η_{max}. However, it is obvious that compared to the conventional

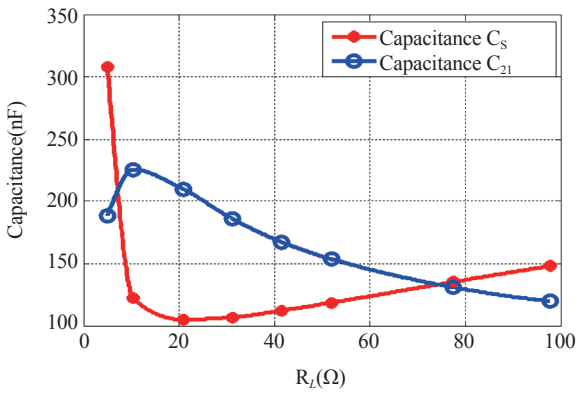


Fig. 17. The capacitors value and R_{21} at different actual load R_L conditions.

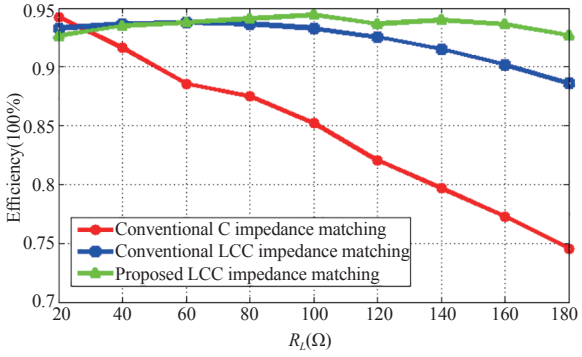


Fig. 18. The transmission efficiency η at different actual load R_L conditions.

impedance matching methods, the efficiency of the proposed impedance matching method is higher for different values of R_L, especially those far away from the optimum value.

B. 3.3 kW WPT System for EV Charging

The proposed LCC impedance matching method is applied to designing wireless charging system for electrical vehicle(EV), which can transfer 3.3 kW power over 20 cm distance. The coil subsystem of EV wireless charging system contains magnetic disk, coil layer and steel plate, as Fig. 19 shows. The steel plate is used to mimic the eddy current effect of EV chassis on coil. The magnetic disk adopts silicon steel sheet, which can not only decrease the eddy current loss, but also improve the quality factor and coupling coefficient.

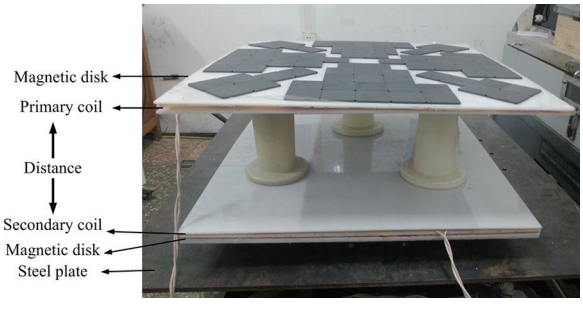


Fig. 19. Photo of wireless charging system.

Both primary and secondary coil is the same sizes, and wound by Litz line, as Fig. 20(a) shows.

(a) coil wounded by Litz (b) experiment result

Fig. 20. Coil and experiment result.

In our system, the battery is charging from 320 V to 350 V. When charging at the normal power, the charging voltage is 336 V, the charging current is about 9.8 A, and the equivalent R_L is about 34 Ω. Thus the secondary side parameters can be determined. Even more, primary side circuit parameters can be theoretically computed to meet the nominal power output after calculating the equivalent impedance of secondary side in TABLE II. WT1800 power analyzer is used to measure the system efficiency (end to end efficiency), as Fig. 20(b) shows, where Urm3, Irm3 and P3 are the input voltage, current and power, while Urm4, Irm4 and P4 are the output voltage, current and power, and η1 is the system efficiency. It can be seen that the system efficiency is about 92.7%.

TABLE II
WIRELESS CHARGING SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
L_{10}	67.7 *uH*	L_{21}	86.1 *uH*
C_{10}	266.6 nF	C_s	112.75 nF
C_{12}	86.3 nF	C_{21}	175.7 nF
R_L	34 Ω	Coil Size	40 cm*40 cm

VI. CONCLUSION

This paper theoretically analyze the operation mechanical of secondary side LCC circuit under rectifier load, and then investigates the equivalent complex impedance calculation method for rectifier load, which is significant for theoretical designing to satisfy the maximum efficiency and normal power output. The proposed LCC impedance matching method can effectively improve transfer efficiency, especially when R_L is far away from optimum value. Typical WPT system researched in this paper, the optimum value of R_L is about 12 Ω, and the transfer efficiency gets the maximum value 97.2% without LCC impedance matching circuit. If $R_L \neq R_{opt}$, WPT system transfer efficiency with LCC impedance matching is obviously higher than the typical one. When $R_L > 30$ Ω, transfer efficiency with LCC is about 2% higher, and When $R_L > 60$ Ω, transfer efficiency with LCC is about 4% higher.

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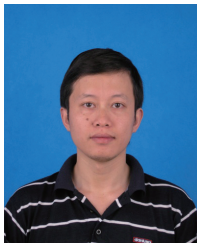

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CPSS TRANSACTIONS ON
POWER ELECTRONICS AND APPLICATIONS

(Quarterly, Started in 2016)

Vol.2 No.3 Sept. 30, 2017

Sponsored by: China Power Supply Society (CPSS)

Technically Co-Sponsored by: IEEE Power Electronics Society (IEEE PELS)

Supported by: Sungrow Power Supply Co., Ltd.
Xiamen Kehua Hengsheng Co., Ltd.
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Editor-in-Chief: Jinjun Liu

Published by: Editorial Office of CPSS TPEA

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